

**Date – 04/19/2011**

**Attendees:** CJ Clark, Bill Tuthill, Brian Turmelle, Carl Barnhart, Carol Pyron, Craig Stephan, Ken Parker, Roland Latvala , Wim Driessen, Francisco Russi, John Braden, Dave Dubberke, Heiko Ehrenberg,

**Missing with pre-excuse** Adam Cron, Ted Cleggett, Adam Ley,

**Missing:** Lee Whetsel, Neil Jacobson, Bill Eklow, Ted Eaton, Mike Richetti,

**Agenda:**

- 1) Patent Slides and Rules of Etiquette
- 2) **11:05 Clause 9 and 11**
  - a. Wrap-up3)
- 3) **11:30 PDL Annex C - Review Discussion**
- 4) **11:45 New Business – BSR Segmentation**

**Meeting Called to order at 11:05 am EST**

**Minutes:**

Review Patent Slide – Reminder sent out over email during the last week.  
Review of Working Group Meeting Guidelines

Clause 9

Carol suggests removing the word “snippet” and use a more formal word.

CJ: don't use Reset\* in figure 9-3 since it is not the output of the tap and people might grab the figure and use it incorrectly.

Carl: there is a note in section that describes Reset\*

CJ asks if the group has looked at it.

Ken and Heiko have looked in depth but rest of the group has not thoroughly gone through the section.

Carl asks if we should postpone adopting the changes.

Carol would like to move forward

**Carl moves to adopt changes made in clause 9 without prejudice to future changes with the modifications we heard verbally**

**Ken Seconds**

**No discussion related to motion**

**No objections**

**Motion passes**

CJ wants to discuss how a Vendor's IP is going to plug on their TDRs. Should we make standardize on a specific interface

Would like to see only 3 signals routed.

Doesn't want to add the AND gates for every TDR as shown in Figure 9-4.

Wants to interface at ShiftTdrBit,CaptureTdrBit,UpdateTdrBit rather than

ShiftDR, CaptureDR, UpdateDRState is the “TAP interface”.

Francisco: Logic outside register (9-4) is usually decoded somewhere else and not part of the IP that is delivered.

Carol: that logic is back in the tap controller

Francisco: correct. back in the tap controller or decoded somewhere else

Carol : typically at some common global point

Carol: this method is done this way already. Clock gating and select gating in a common global point. Could be in the tap but doesn't have to be.

Francisco notes that the only signal that shouldn't be gated is the reset signal

Carol: doesn't have a problem with the figures. To make the figure clearer to the ready we could put a dotted box around the AND gates to show that it is common logic.

Carl: The real issue is what we put in table 9-1 not the figures. What do we define as the TDR interface?

CJ: agrees that the table is where we need to concentrate

Carl: Thinks this is a non-issue. feels that the TCK does the majority of the toggling, but not the other signals. Tap signals are not active after leaving board test/manufacturing. So it is not an issue

CJ: believes that this isn't always the case

Carol: wants to know if this is a rule, recommendation, or going to be an example

Roland: are you implying that figure 9-4 is preferred over 9-3. What is the advantage of 9-4?

CJ: compatible with 1500 and 1687. No gated clock. Inputs from members to use state base method. Real issue is what we want IP vendors to provide. Gating signals local to IP or global to all IP

Roland: uses gated clocks and would have rethink how to do things with this table and states

Carl: state decode and table is closer to what people are doing

John: leave table 9-1 as is and leave it to the designer to do what is best for his design.

CJ: can't leave it to the designer on this one. Trying to specify what the IP vendor uses as an interface and the IP vendor and Designers may not be in sync.

Francisco: figure shows gates outside the dotted line and feels that is indication how the vendors are to deliver the TRD block.

CJ: points out that table 9-1 says differently than the figures show

Carl: in the figures, the dotted line is describing that this is showing the individual bit of the TDR

Carol: was not the original interpretation of the figures and now understands CJ's concern better

John: doesn't see a problem with the way the recommendation is currently written.

CJ: wants to make sure the recommendation is clear and that if the IP vendor and designer don't talk don't want there to be any confusion

Carol: feels that she can use which ever interface that an IP vendor gives her and be able to deal with the power or SI issues if needed.

Carol also points out that the IP provider may want all 4 signals to come to their TDR block to be in “control of their own destiny”.

Carl: feels that the 4 pin interface is more flexible and gives the vendor and the design tools more options. If we force people to use the 3 wire option it may cause more problems for the tools to optimize the code.

CJ: sees it differently, as an IP provider.

Carol: feels that we should make the interface a recommendation and not a rule.

Discussion will be taken off line and into email

Due to time limits, Francisco was not able to present his new business

Francisco's New business will be first order of business on Friday's meeting

CJ asks Carl to put latest draft version on the web after accepting changes in Clause 9

**Meeting adjourned: 12:00 EST.**

**Next Meeting:** 4/26/2011 11:00 AM EST

1 Motion Made

**Motion to accept changes to date on clause 9 without prejudice to changes in the future.**

**Motion Passed Unanimously**

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**[JOIN the meeting as GUEST](#) – will have to ask to present**

Meeting time: Tuesdays 11:00 AM (EST) (Recurring)

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### Current Issues listed and who will champion that issue.

1. Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

### Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components

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- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.