IEEE 1149.1 Boundary Scan Working Group Minutes

Date – 6/1/2010

Attendees: CJ Clark, Bill Tuthill, Adam Ley, Dave Dubberke, Carol Pyron, Wim Driessen, Francisco Russi, Heiko Ehrenberg,

Missing with pre-excuse: Carl Barnhart, Roland Latvala, Adam Cron,

Missing: Bill Eklow, Ken Parker, Ted Eaton

Agenda:
        Continue to refine INIT

Minutes:

Update on status of INIT from Friday's init meeting.
        When INIT requires external resources are necessary such as system clock our plan is to craft the rules such that those external resources will need observation in the INIT Status register.

Wim – Looking at the May version of INIT.   Should we make the rules more general for other standards instructions? Lines 69/70 of INIT rules from Carl
Carol – not going to define anything outside 1149.1. Intended to affect other standards that reference 1149.1 but can't list all instructions.
CJ – will try to improve a little bit if possible. Can't call out other instructions in other standards.
Carol- Was there a final consensus on status bits/register?
CJ – the general consensus was that we need a status register and that it needs to be mandatory.   There should be a status bit for anything that requires an external resource to perform the init sequence.
Carol – CE pins having OO cells. Could say that this type of initializing OO is in status rather than the boundary register.
CJ – seems to be the way we are heading. That would be preferred method
Carol – having the CE like this wouldn't give a pass/fail indication, but would give a indication if the CE pins were set correctly for the activity of the IC.
CJ – need to allow a person to make choices that are correct. Don't have to decode certain combinations that are not legal combinations.
CJ – moving towards having status in order to diagnose. If the tools can't back into what the problem was, there is little advantage to 1149.1 in the field.
Carol – need to allow for flexibility to be future proof in describing categories for what is required status.
CJ – won't be too helpful if we have a lot of setup features in the board test. (1149.1 addresses this area).
CJ –need a method to guarantee that we are initializing important features for EXTEST to work that they are observable. We don't know what could happen especially out in the field that could impede that operation. Understanding what the failure was is important.
Carol- worried about features that would be thrown in to the nice to have category.

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CJ – want to set bits that we can observe. To make sure that the operation in the chip is occurring when a certain init sequence is called.

Carol – this is part of component test.   It has assured you that if you set the bit the correct action has taken place.

CJ – correct only if it is something that doesn't require an external resource.

Francisco - regarding earlier conversation on One Hot – it is difficult to build register if it is many bits. Is one hot good for status register if it is very large?

CJ – The one hot implementation was for the setup register.

Francisco - regarding the status register in general – are we going to monitor every operation with status register internally that is going to be setup with the init instruction

CJ – no

Francisco – if we have different actions from init setup (i.e. 6 or 7 I/Os that have 3 different settings.) This will determine the minimum length of status register?

CJ – need sufficient bits of status to guarantee correct operation before going into EXTEST.

Francisco – minimum number of status bits? Is it up to user?

CJ – yes within the rules of standard.

Francisco – is this "rule" captured?

CJ – this is part of the refinement state of the rules. Rules May be more strict than what we have now. Need to have enough status to Develop, debug, and diagnose using the tap.

Wim – why don't you have small status register?   Or-ing many of the status bits to a single bit for ease of reading.

CJ – if you require a lot of external resources to do init, than breaking it down to a small subset of bits wouldn't allow you to do any diagnostics on board. Really need to get to a 1 to 1 correspondence to external resources. If the things are not external to the chip than you could or/and them all to 1 bit to indicate status.

Francisco – compress status to master fail bit so you can look at just one bit and then expand to other bits in status register if there was a failure.

CJ – there is no advantage to having a single bit to tell if the one or more of the status bits are failing because we read (scan out) all of the status bits in the register. Can't just read the one single status by itself.

Meeting adjourned early due to no new business for INIT and several people missing from the meeting.

Meeting adjourned: 11:47 AM EST.

Next Meeting: 11:00 AM EST

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

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1   Observe only. –   Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:
- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.