

Date – 6/22/2010

Attendees: CJ Clark, Bill Tuthill, Adam Cron, Ted Eaton, Carl Barnhart, Wim Driessen, Francisco Russi, Dave Dubberke, Carol Pyron, Heiko Ehrenberg,

Missing with pre-excuse:

Missing: Bill Eklow, Adam Ley, Roland Latvala, Ken Parker,

Agenda:

- 1) Wrap up on unconnected pins (additional input/concerns if any)
- 2) Work on defining new pin class for INIT, these are pins not in the boundary register.
- 3) Refinement of INIT types
- 4) Beat up on editor for too slow progress – So last week DAC, this week tight deadline for Wed morning.

Minutes:

Meeting called to order at 11:03

No-Connects.

Bill Bruce is concerned about 2 cases.

No Connects that are connected – Designer just doesn't want to have the pin in the test.

Chip in multiple packages, internal signal that tells what the logic is, such a signal would be depowered associated with unconnected pads. Except if you have a BC9 or BC10 that monitors pad. Simple Output2. If pin is connected in bonding and not connected on board you get a different result if IO is powered down. And creates an inconsistent behavior for ATPG . (power down is main point of this case)

Rule if package pin is disconnected any associated BS cell should be treated as internal.

Francisco – effort was to disconnect internal cells from no-connect cells.

Carl – standard says that no-connect cells have no parallel in or parallel out.

CJ – effort with the * is important effort. Difficult to change BS cells to match as internal when these situations occur. This will probably occur more in the 3D domain.

When you get to 3D package and want to do ATPG in 3D environment, fall short in features and capabilities that are needed. The ability to associate domains of power.

Carol – unconnected pins in package - having expectX on anything that is * is fine.

3D- not relevant topic for dot 1. beyond the scope. Not board interconnect.

CJ – 1149.1 has a **Test Access Port**. This is a standard for Test. Not just board interconnect. . There is a lot of stuff done with 1149.1 beyond just toggling pins of chips.

Carl – is happy with statement that associated BS cells capture undefined data when pad is not connected

IEEE 1149.1 Boundary Scan Working Group Minutes

Should make it clear that it is non-compliant to call a pin not connected if it is connected inside the package.

Ted – won't we just call it an Analog pin to get around it to make it compliant?

CJ – Right. Still have class of linkage pins.

Carl – no way to detect pin connected in package

Ted – most of ATPG tools will record an error if it sees a pin that is not in the package file.

Carl – what do we return when it captures? Undefined data?

CJ – Yes, that is the easy route. Not helping much for people wanting to do validation. Can run a different package though. Have some concern we are ignoring industry trends.

Carl – what we define as No Connect is still a no-connect in a 3D stack. Not sure we are ignoring 3D stacks.

Carl – is it legal for a pin to be a no-connect in all packages

CJ – allowed having 1 or more port maps that don't have pins connected.

Carol – agrees with point.

Carl – no requirement that an unconnected pin be in any port map

CJ – Yes.

CJ – back to the 3D stack. Little different. Would like to know that you can scan through these particular BS registers. Maybe you don't use the "*" for the pin map. Have redundancy and other issues in stack. Might add some complexity.

Francisco – power down segment on chain. Have a way in the standard to partition a register. May expand to chain for power down.

CJ – may need a proposal. Some BSDL architecture change required. What are the benefits?

CJ – would like to see multiple TAPS addressed in 1149.1

Carol – had multiple taps on die for a long time without being standardized. Was not set as something to work on in the group.

CJ – would be nice to solve this problem. Problem has been around for a while and may be time to address it to help with the 3D initiative.

Ted – has a chip with 9 TAP controllers. 1687 is going far enough to hook up the TAP controllers. But doesn't have an association to any boundary scan register.

No-Connection Action Summary –

Add to standard to make clear any and all pin map can have no connect. Port doesn't have to be mapped out

Add Note - May not capture same data (X) on No-Connect pins

Rule that pin is present you shall not call it a No-Connect

Carl withdrew comments about internal cells not having a pi/po

- is the additional pinmap showing that you can have a pin name or * * to denote you don't have a connected boundary scan register.

INIT

Carol – comments from Example 3 of BSDL.

TDI/TDO was thrown in as a place holder

CJ – INIT Types. Break down categories of INIT. Not TDI TDO type

CJ – new pin class.

Potential input description.

Have pins that are now part of the init function. Might be voltage being set for receiver. Could be digital pins, pins that are involved in the INIT process that can be monitored in the INIT DATA register. Would not be in the boundary register.

Carol – New class.. not power pins, not linkage pins.

CJ – bigger problem is where are the things that people might do to abuse the standard.

Carol – that is a concern.

Carl- rule that those pins need to be captured in one of the INIT register. Pins need to be observed.

Ted – only digital pins not analog.

CJ – digital input pins.

Ted- wouldn't you also want to observe during an interconnect test.. Should they be in the boundary register?

CJ – should we require the

Carol – can not participate in EXTEST and cannot be driven to a value. Could be observed in boundary register.

CJ – input only??

Carol – yes.

CJ – Would prefer that they be in both.

Carol – don't want any other chip on the board to try and toggle these pins.

CJ – we don't define ATPG.

Carol – need to give a clue to the tools to tell them not to mess with them. Do this with a pin class.

Ted – how many of these pins exist? When is it impossible to get to the INIT Data Register due to constraints?

Carol – don't see too much of a problem with that.

CJ – what is useful is that we brought out Board/Init definition.

Still could be in boundary register and wouldn't have to create as many rules and exception.

Ted – INITDATA register can be the boundary scan register.

CJ – yes.

CJ – control or initialization for the board section. Pins that are being observed for INIT would also appear in the Boundary Register.

Ted – wouldn't I need to know that my compliance pins were pulled correctly for initialization? Do we need different classes? Can we call them compliance enables?

Carl – do we want to expand the formal definition of Compliance Enable? Voltage selects violate the standard. If in Boundary Register they are optional redundant observe only.

Carol – yes observe only cell. Simpler solution may be to redefine Compliance Enable

CJ – Changing the definition of Compliance Enable would be easy to do.

IEEE 1149.1 Boundary Scan Working Group Minutes

Carl – only talking about pins that are needed for INIT. Should we expand the definition of Compliance Enable to describe those pins? Or create a new class? Not worth making a new class.

CJ- Clock in this class? Can it be defined by Compliance enable?

CJ – ok if we are referring to INIT pins.

Carol – what if it is TCK . How do we know that TCK is running?

Ted – shift a scan register.

Carol – many reasons for failure might not be TCK.

CJ – if there is no one arguing for systemclocks for initialization maybe it is not important.

Ted – would have to ask others.. People do use the system clock.

Carl – would object to removing SystemClocks.

Carol – don't use SystemClocks. Do things with TCK.

CJ – do require some method that they are active and doing something.

Carol – do we require or nice to have?

Ted – nice to have but should not be required.

CJ – pins that we want to observe. INIT DATA is more than just putting data in. pins we want to observe before we get to the Run state.

Ted – don't want to have a counter on all my clocks and running all the time

Carol – if you need a sysclock you can allow polling of INIT STATUS register. People could provide visibility to show that at what state the process is at.

CJ – can't be required to show stage.

Carol – no, but would be good design practice.

CJ – if you just had the status that it is initializing or not. And have 100 different differential clocks you can't diagnose what is happening.

Ted – what is going to tell counter to start. What is going to do the required clock musing. How are we going to monitor it all in the same init data scan? Do I have to poll?

Carol – Init Status register will tell you the state of the state machine.

Ted – I

Carol - INIT DATA is to capture static values on a certain class of pins

Carol – the only way to know your pins are right is to do a true EXTEST.

CJ – there were some concerns to go through multiple runs.

CJ – are there situations in your environment that could cause damage to your chip?

Ted – don't even see the voltage range of possible configurations as to be a problem.

CJ – carol has a silicon insulator. Have voltage could be higher

Ted – at some point the current could get high and break the chip.

CJ – that is one class.. they we have another class that will cause initialization to not correctly be applied.

CJ – complexity is exasperated because we won't draw a line

CJ – Rule – need to tie into the design and designers that would not allow TCK for initialization. Not getting a strong care about that this is a problem.

Ted – don't know whole industry. Would like to write rules as TCK is only clock and allow systemClock and have some way to monitor that it is running.

IEEE 1149.1 Boundary Scan Working Group Minutes

Ted – can't capture in INITDATA register because you have to turn it on before you can capture.

CJ – makes a requirement to capture it in INIT STATUS register.

Ted – Can be in INITDATA but will have to scan it twice.

CJ – don't see a problem with scanning more than once.

Cj – still see hole to be closed up in INIT.

CJ – can't accommodate everyone in industry. Need to predict what is in the future and try and support 85% of the market place.

Ted – as soon as you allow multiple scans and systemclocks you are enabling all sorts of complex operations. Carol is right to keep it close together to keep it from being a mess.

CJ – leaning towards TCK as clock for initialization. Makes rules clearer and removes confusion.

Ted – need to be careful writing rules. TCK is the clock but allow systemclock and provide status. Not sure where the difficulty is.

Carl – agrees with Ted but wants to capture static values and monitor Systemclock. Makes systemclock use more expensive and move towards using TCK.

Meeting adjourned: 12:38EST.

Next Meeting: 11:00am EST

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

1. Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1

IEEE 1149.1 Boundary Scan Working Group Minutes

- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.