

Date – 8/10/2070

Attendees: CJ Clark, Bill Tuthill, Craig Stephan, Ken Parker, Dave Dubberke, Carl Barnhart, Adam Ley, Brian Turmelle, Carol Pyron, Francisco Russi, Roland Latvala, Neil Jacobson, Wim Driessen,

Missing with pre-excuse:

Missing: Bill Eklow, Ted Eaton, Adam Cron, Heiko Ehrenberg,

Agenda:

Review the latest on BSDL extensions from Friday's Tiger Team Meeting

Minutes: called to order at 11:04

Update from tiger team on Friday

Ken, Carl, Carol met on Friday

Reviewed BNF and sent out updates to Tiger Team + CJ

Ken presented the document - Basic Structure of Data Register Description

The document was worked on during Friday's tiger team.

New attributes needed

Register_Mnemonics

Register_Segments

Register_fields

Port_Associations

User Packages

Embed mnemonics and segments in this package

Information tag

“info<comment information> “

Carl – can't user a “ in an info tag because it would close the string.

Comment information can not contain a “

Can split tag across line boundaries using a &

CJ – cannot format with a carriage return?

Ken – correct. This is not supported. Not much need as the comments are meant to be short.

REGISTER_MNEMONICS

Syntax

mnemonics

attribute REGISTER_MNEMONICS of <component name> :entity is
<register mnemonics string>;

For use in user package

attribute REGISTER_MNEMONICS of <package name> :package is
<register mnemonics string>;

Use of others keyword to represent all unnamed patters not enumerated in earlier elements.

Semantic Rules

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Descriptions of mnemonic name, bit field names, patterns

Patterns can contain X

All patterns and pattern shorthand elements that appear in a <named bit fields list> shall have the same length

Others keyword cannot be used when all possible patterns have been enumerated or implied

Additional information can be found in document that Ken emailed out

In Ken's example the mnemonics all start with an Alpha character.

All BSDL identifiers need an Alpha character.

CJ finds this unnecessary as a mnemonic

Ken – strict rules as a VHDL identifier

CJ – is this an identifier? It is really a text string.

Carol – believes that it is an identifier

CJ – after the (the first thing is a string

Ken – doesn't feel that this is a "cut and dry" matter since you don't know what the intent is after the (

CJ – doesn't feel that anyone is going to be parsing that information string.

Adam L – The names will be used as identifiers in the PDL. So they would need to conform to the rules of identifiers in PDL context.

Carl – used as identifiers elsewhere in the BSDL and will be parsed. Chosen to use the same rules for the identifiers in the string as outside.

Adam L – needs to be rationalized against the PDL.

CJ – our PDL is operating on what is found in the BSDL. Wouldn't expect that PDL that was written for 1149.1 would not run against something that was made for 1678

REGISTER_FIELDS (section needs more work and is where the tiger team left off)

Ken describes the syntax for this attribute.

Carl – integers can be positive or negative. VHDL provides a positive type that will always be positive. Register length can't be negative and could be a possible problem with using "integer"

Ken – integer is defined to be unsigned per B.6.2b Lexical Atoms

Carl – asks about hierarchy. 1687 does not define hierarchy yet and where does that leave 1149.1 for PDL?

CJ – examples show the use of a dotted path to support hierarchy in 1687 PDL

CJ – array however is not included in 1687 BNF for PDL

Ken – only 2 mnemonic assignments can be made. Each assignment needs a unique direction (iread/iwrite)

CJ – array of registers seems new. Is there confusion in the parsing when defining an array of channels versus indexing to a specific bit of channel?

Carl doesn't think so

Carl – simple register and array both have () which could cause confusion.

*Carl – it's the : that makes the difference. It is the use of the : that says that it is an array.

CJ – can't index into a single bit?

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Carl – has no real meaning in the BSDL. In the PDL you would address it as the single bit.

CJ – Am I allowed to call out individual bits of a register that is inside of a package or am I restricted to calling out the entire register?

Carl – you can at least go to sub field definitions. So yes you should address the individual bits.

CJ is concerned about the definition of the register array is not unique enough for a parser. The syntax does not differentiate when talking about bits in a register and talking about number of elements. Concerned about some possible collision due to the syntax

Ken will send out email containing his Basic Structure of Data Register Description that was presented.

Do we want this presented to the 1687 group?

Carl – it is a little premature

CJ – agrees

Carol – should give them a head up.

Roland- segment array's bit order is still MSB to LSB?

Ken – will need to define that carefully when defining segment array range.

*Carol will be on vacation Friday (8/13).

Meeting adjourned: 12:00 EST.

Next Meeting: 8/17/2010 11:00AM EST

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

1. Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

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- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.