

Date – 10/26/2010

Attendees: : CJ Clark, Bill Tuthill, Ken Parker, Craig Stephan, Carl Barnhart, Brian Turmelle, Wim Driessen, Dave Dubberke, Adam Cron, Carol Pyron, Adam Ley, Francisco Russi,

Missing with pre-excuse Heiko Ehrenberg,

Missing: Roland Latvala, Lee Whetsel, Ted Eaton, Neil Jacobson, Bill Eklow,

Agenda:

- 1) Input from Wim on his b-s cell proposal
- 2) Input from Ken and others on init-clamp
- 3) Further input on IC_Reset

Meeting Called to order at 11:00 am EST

Minutes:

Input from Wim on his b-s cell proposal
Review of slide sent by Wim

Clamp_hold target register is boundary register

In normal mission mode the clamp ff takes over

Adam – still need the ClampHold functionality as well?

Wim – still need to remember that ClampHold is Active

B-s is still boundary scan and can take over control.

Carol – why having update flow and clamp hold flop. What is advantage?

Wim – update ff follows normal rules. Capture ff is reset under normal rules.

If ClampHold remains active the clamp ff controls the

ClampHold is not cleared by normal reset activities from BS

Carol – block reset and clearing Boundary Register from TLR

CJ – blocking the reset out of the tap controller

Wim – this is a way of having control over PI instead of messing up the rules of boundary scan.

Traditional tools can still use Boundary scan as usual

Adam – seems like tradeoff between or gates back at the TAP vs. an extra flop at every pin

From a Black Box stand point can you find out you did this?

Wim – it is either this method or something else and not both.

Carol – from an external point of view can you tell if this is the implementation?

Adam – when you violate some rule if you did it this way.

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CJ – you wouldn't know because you would have to shift the data. This ClampHold flop is similar to what you do for fault injection

2 scenarios:

- 1- Everything is in the TAP and the reset is distributed to all the boundary register. This method decentralizes from the TAP and provides local control.
- 2- Other method is to add 3 extra signals that need to be routed and extra flip flop. This approach might slow down the adoption.

What Wim is trying to do is resolve a problem where JTAG tools will need to be changed to understand Clamp Hold.

KPP – only 2 new signals that are being added (CJ's scenario 2)

Carol – will preload update this register?

Wim – no

Carol - At update IR of ClampHold what is driving the pin

Adam C - Need a ClampLoad and ClampHold

Wim – this is like an initialization instruction

Adam C – don't see where this is saving in the Tool

Wim – The first step can be loading clamp and last step is to release clamp and steps in between don't know that Clamp has been done. This keeps current tests from having to be rewritten to support ClampHold.

Carl – Mode signal would have priority and switch out of Clamp mode?

Wim – do need to go back to clampholdActive and set back to normal mode.

Ken – This would be an extra latch in every Cell.

CJ – We will have to sell this idea to the design community.

CJ – Lets continue this discussion off line to give some time to Ken and his issues. We can cover more ground on the reflector

Ken's input on INIT-Clamp

Review of email and design that Ken sent out in email

Define register opcodes to avoid Single Event Upset so that it takes two bits to change to get from Bypass or IDCODE to EXTEST

Clamp Hold pushed back into the TAP and no extra wires

Ken – Circuit does not use decode of IDCODE or BYPASS except for ICRESET to clear sticky bit.

Carol – IC reset is implemented. What happens if it is not?

Ken – has to offer concept as way to set it and some way to clear it. And that means if there is only to clear it with ICRESET than you can't have ClampHold pair.

CJ – want ClampHold ClampRelease pair.

Carol – ok. That is required.

Ken – Carol thinks of ClampReset is apart from ClampRelease

CJ – if you run ClampHold there are times when you want to Reset the logic inside

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Carol – put the ICRESET question to the side.

CJ – want to have ClampHold and ClampRelease as a pair. Two different things:
to do reset
release the ClampHold

Ken – the delay flip flop is more than you need?

Carol – 2 flops in parallel. 3 flops are good but may be extra. Should be able to ensure against SEU's without requiring multiple clocks.

Ken – mode line when CH or CR is present in IR would be set to 1. So memory stuff only has an effect when you replace CH CR with a new Instruction.

Ken – AR – to redraw picture with updates made from Carol, CJ, and Adam

Carol – need to define what IC RESET does before we put in diagram

CJ – Clamp Release is better in the diagram while we figure out what ClampReset is. We should consider divorcing the two (release and reset)

CJ – need to think of the other release options.

Want to leave current instructions the way they are.

Not sure of the reason why ClampHold work through BYPASS, ID, HIGHZ

Carl – want ClampHold to only be effective for user instructions.

CJ – yes

Carl – or by other instructions created by Dot6.

CJ – want to preserve current 1149.1 Instructions mostly for the 20+ years of training people have. People out there that know that Bypass puts the chip back in mission mode.

Adam L – sympathize with Ken's position, being that point of clamp hold is there is a need to coordinate the return to some semblance of a mission mode that has at least the possibility of being safe. That requires there be a coupling between the ICRESET and ClampRelease. ICRESET is parameterized and one of the bits could be doing reset in ClampHold or not

CJ – what do we want to do with predefined instructions that we have today and what are the benefits of changing them.

Ken – would like to control when things get lobotomized and have an automated way of resetting and rebooting boards. Don't want to leave boards in a lobotomized state.

When tests complete they go through TLR.

With ClampHold you can control what is happening with the chip until it is made to go away.

Carl - why today don't you load clamp instruction and go into bypass and wait.

Ken – not every chip has a clamp instruction

Carl – if you issue a TRST ClampHold goes away. Most everything can be done in CLAMP. Don't see where you have gained with ClampHold over a different usage over instructions that exist

Carol – ok maybe for board test, but not when you need to strap chips for 1687

Carl – all we need to do is add an instruction to force Clamp and version that doesn't force Clamp.

CJ – problem is that granularity isn't there. Difficult for designer to come up and partition the scan chain.

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Need a method that doesn't depend on the way the designer builds the chip. This will help the end user

CJ – is there an advantage to have Clamp pervasive through standard instructions. What does that mean for designers and users?

Carl – invasive instructions would be INIT_RUN, EXTEST, INTEST, HIGHZ, CLAMP already specify behavior of IO. They should behave as defined but when they are no longer the active instruction ClampHold should still be there.

CJ - good point. It would be nice to leave sticky behavior there.

Carl – non invasive instructions – IDCODE, BYPASS, PRELOAD, SAMPLE, INIT_SETUP

Carl – do we preserve the TLR or the instruction?

Carl – Need a good definition of Test Mode

CJ – heading towards pervasive. Need to understand the ICRESET vs. ClampHold/ClampRelease need

Meeting adjourned: 12:00 EST.

Next Meeting: 11/9/2010 11:00 AM EST

NOTES:

ITC meetings

Public meeting at 10:30-11:30am on 11/2

Power Session at 6-8PM on 11/2

Meeting for 11/2 is canceled

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

- 1 Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

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- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.

Weekly 1149.1 Meeting coordinates

1. Please join my meeting.

<https://www1.gotomeeting.com/join/172495048>

United States: +1 516 453 0012

Meeting ID: 172-495-048

Audio PIN: Shown after joining the meeting

2. Other call in numbers

Australia: +61 (0) 8 6365 4094

Canada: +1 416 800 9290

Germany: +49 (0) 898 7806 6462

Netherlands: +31 (0) 208 080 380

Sweden: +46 (0) 852 503 470

United Kingdom: +44 (0) 203 051 4835