

Date – 01/04/2011

Attendees: CJ Clark, Bill Tuthill, Dave Dubberke, Mike Richettie, Adam Ley, Carl Barnhart, Adam Cron, Craig Stephan, Carol Pyron, Brian Turmelle, Wim Driessen, Ken Parker, Roland Latvala, Ted Eaton, Francisco Russi, John Braden, Bill Eklow

Missing with pre-excuse

Missing: Lee Whetsel, Neil Jacobson, Heiko Ehrenberg,

Agenda:

- 1) Required Patent Disclosure Slides
- 2) Review/Discuss IC_RESET
 - a. *Review 3 visio slides which will be used to kick off discussion on finalizing some details on IC_RESET.*
- 3) Editor Status
- 4) New Business

Meeting Called to order at 11:01 am EST

Minutes:

Reviewed Patent Disclosure Slide

IC_RESET

Review of CJ's first slide

Carl: In the last meeting it was agreed to drop clearing the TDR with RunTestIdle.

Going with programmable resets.

CJ: Currently it looks like it is clearing in Test Logic Reset.

Carl: has not updated the figures yet for reset

CJ: Proposing TRST pin used for clearing register and not every time you enter Test Logic Reset.

Problem.. What do you do with the Reset Pin and how to manage it?

Use ClampHold to keep RESET from toggling. Could be burdensome for the designer.

Slide 3

Final solution

If we set register bits to 1 will make controlling resets easier.

Don't want to mandate having Clamp Hold to make reset work.

Have one master bit that controls the reset to be either on chip control or JTAG.

Carol: won't know what state you are in until TRST.

Placing the TRST/POR higher priority than the system reset

Carol: putting more JTAG in the way of POR. May cause some opposition from designers.

Ted: does not feel that is going to be a problem.

Carl: Active high or active low. Responsibility of the chip designer. Should not be part of the spec. External should look the same.

Standard should define an instruction and a register. And downstream logic should be up to the designer.

Adam C: define 1 as reset and 0 is not. After that it is the designer's responsibility how it is used in the chip.

Carl: standard says what goes in as TDI and what comes out as TDO. Not what the value of the set and clear are.

Carol: agrees with Carl.

CJ: does not agree. Wants to have consistent approaches. Especially for instructions that we are defining. Rather than leaving to the designer.

Should have more of a structured approach for the end user community.

Will not mandate how the decode logic is done.

Adam C: Reset Pin would not be able to come in without being touched

CJ: true. Couldn't not be pulled directly into chip

Carl: why not?

Carol: clamp hold only affects outputs not inputs.

KPP: inputs too

CJ: Clamp Hold impossible to implement by bring system reset into the chip unimpeded.

Carl: doesn't agree. Have to bring in SystemReset where it isn't blocked by any register. Will have a BC4 on it. Has to be controlled on board.

Ted: This is against our goal. Our goal is to allow the TDRs to bring the chip up into a state regardless of what is going on with the board reset.

CJ: Can't guarantee to make the IC_RESET work because the system reset is not under control. Goal of IC_RESET is a JTAG based IC reset. Why? Because we don't have control of the system reset pin. This is a Catch 22 – trying to implement IC_RESET so we can control the IC_RESET with JTAG only. If we have an OR than we have to be able to control the system reset. If we can control the system reset pin than we don't need IC_RESET. The problem we are solving is a JTAG based reset that allows us to control reset on the chip in different domains regardless of the system reset state.

Adam L: has a point of order. Adam feels it is difficult to moderate a discussion that you are key to. Adam suggests that CJ should recuse himself as chair during the discussion and allow Carol to moderate

CJ: Feels that Carol is part of the discussion as well. CJ will recuse himself if the discussion gets more contentious

Carl: Feels that CJ is making an assumption of an uncontrolled system reset. This is a wrong assumption. Could be multiple system resets coming in going to the ORs shown in the diagram.

“In Control” means that it may simply be controlled to a known value. The OR condition is an acceptable way to allow JTAG to add a finer control. IC_RESET through JTAG was always an OR function of what the RESET pins are.

John B: reason for IC_RESET is to get rid of Zombie like state before we return control. If we have a BC1 type cell we have control over the reset pin.

CJ: want to be able to put chip into reset. Correct if you have BC1 type cell that could drive that. But not always guaranteed. When operating INITSETUP we need control over RESET. And might want to reset logic before running test.

Carol: Clamp Hold – Gating of system reset is restricted to INIT DATA reset. That is different than blocking system reset to the rest of the chip

And is only needed if you want to share your INIT_DATA domain with the TCK domain

CJ: if TRST on the left hand side doesn't occur than you have part of the chip that is

Carol: there is order of precedence in the RESETS. There are possible contention points in a chip that you need to block by the order of resets. Some of IP busses there are requirements for things to happen after Reset.

CJ: more comfortable with slide 2 rather than slide 3?

Carol: yes.

CJ: will redesign slide 3 to make it function more like slide 2 regarding the SystemReset propagating through decode logic while register is at X state.

Ted: what if there is an open on TRST?

Carol: in the hardware spec that specifically to wire up TRST and SystemReset. There is a pull high on the TRST

Ted: an open will keep the circuit from booting?

Carol: yes.

Carol: agreed with Carl that either you reset the part with the pin or the TDR. Never said anything about blocking system reset

Ken : SysetmReset pin is effectively blocked with EXTEST.

Carol: yes.. EXTEST by definition has higher priority depending on the Cell

CJ: do we want to mandate a particular cell on reset?

Carol: doesn't think we should.

Carl: an x does not propagate through if internal TDR is driving a 0

John; agrees with Carl. External reset is immaterial with TDR at 0

Ted: sees both sides. Resets are tricky.

Feels the issue comes down to the question of “what is our goal?”

CJ: Feels there are 2 goals. A Reset for the chip. A Reset for individual domains

Ted: can we define what we mean by “RESET”?

CJ: being able to bring a chip out of brain dead state and providing a standardized access to controlling on chip's resets through JTAG.

Carol: sees the IC RESET as more of an Or function. . Either reset chip with a pin OR reset individual logic with a TDR

Ted: can you have slide 3 as an option? Ted would use this configuration

Carol: no problem doing it. Just don't want to mandate this design. A Viable option but not the only way of doing it.

Mike R: Would like to see this optional. This is a good idea to have what CJ has on slide 3 as a recommendation to have more control over the system reset.

CJ: maybe that is the compromise position is to not have it mandated.

CJ: only get half the IC_RESET functionality without being able to block SystemReset. Wouldn't be able to manage reset because you can't guarantee reset

Mike: best approach for today is to have this as an option.

Carl: don't want to mandate clearing them at Test Logic Reset.

Carol: are we going to have a standard setting for the polarity?

CJ: would like to put it in the standard

Carl: Test logic reset should not be mandated to change the state of the value in the update flops.

CJ: hasn't heard a reason why Test Logic Reset should change the update flops so it shouldn't be put in the standard.

Only need to clear the update once and that is at power up.

Standard will not say that the update registers will clear at Test Logic Reset.

Meeting adjourned: 12:15 EST.

Next Meeting: 1/11/2011 11:00 AM EST

NOTES:

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

1. Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel

10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.

Weekly 1149.1 Meeting coordinates

1. Please join my meeting.

<https://www1.gotomeeting.com/join/172495048>

United States: +1 516 453 0012

Meeting ID: 172-495-048

Audio PIN: Shown after joining the meeting

2. Other call in numbers

Australia: +61 (0) 8 6365 4094

Canada: +1 416 800 9290

Germany: +49 (0) 898 7806 6462

Netherlands: +31 (0) 208 080 380

Sweden: +46 (0) 852 503 470

United Kingdom: +44 (0) 203 051 4835