Date – 01/11/2011

Attendees: CJ Clark, Bill Tuthill, Adam Cron, Carol Pyron, Brian Turmelle, Wim Driessen, Roland Latvala, , Craig Stephan, Ken Parker, Ted Eaton, Dave Dubberke, Francisco Russi, Carl Barnhart, Heiko Ehrenberg, Bill Eklow,

Missing with pre-excuse

Missing: Mike Richettie, Adam Ley, John Braden, Lee Whetsel, Neil Jacobson,

Agenda:

1) Required Patent Disclosure Slides

2) Reminder on discussion etiquettes.

3) Review/Discuss IC_RESET

- Still in discussion is whether reset-select can combine clamp_hold functionality.

  C & D currently are written as a strawman and require the CLAMP_HOLD instructions to hold the reset-select register values through TLR

- The attached shows how with the single register the same result can be achieved with less logic and without the requirements of CLAMP_HOLD (which are non-trivial). In either case, as written or combining, the ability to hold the reset-select logic through TLR is possible/desired. The question is more of ease of implementation. Is it OK to achieve without needing CLAMP_HOLD. It would be good to have short discussion and a motion?

- Not in the Strawman doc is the option to block the external reset values. This was also discussed where controlling the reset pins is not easily achievable (and the reason IC_RESET is being proposed). This one perhaps is more important with bigger ramifications if not present. Carol had removed her objections. Are there any reasons not to include this? It may make sense to see this in the IC_RESET doc first before motion (if any) voting.

4) Editor Status

5) New Business

Meeting Called to order at 11:05 am EST

Minutes:

Patent Slide shown and reviewed
Reminder of discussion etiquettes
No personal attacks
Let others have a chance to voice their opinion

Carl - Rules c& c don't say Clamp Persistence has to be provided, just what to do if it is
CJ – concern if optional clamp controller isn't provided C&D would set the select register to 1
Ted- doesn't follow why there is a concern
CJ – as written c &c will block when the Clamp Persistence controller is there than reset select register shall be set.
Ted – Doesn't follow why that this one register is so important and others aren't. Would like to see it applied to other registers not just IC Reset
Carl – you're right. Haven't looked at other registers to see how the Clamp Persistence controller affects the registers. Should look at other registers to see if they are needed for other registers.
Carl – disagrees that IC reset is a new idea. Designers have created equivalent instructions for decades. Needs to be careful of definition. Is Test logic reset intended when Clamp Persistence controller isn't there?
Carol –may want to associate in the BSDL each reset pin with its reset block.
Maybe have a reset per pin and an associated blocking bit per pin.
Need to make clear that the resets may not get you back to full operational mode and there is no requirement to doing so.. That it is equivalent to throwing reset pins. This is for the descriptive text
Adam C – do we need to provide local-level and block-level control or have a single reset pin
Carol – that would be up to the programmability. Want to emulate toggling of reset pins
CJ – Need to offer guidance that leans towards understanding in the system environment for blocking resets. Designer may not care but it has bigger ramifications in the system.
Carl – nothing in strawman to preclude that.. it is up to the designer. Reason for Master Reset pin was so that you know that the LSB of the TDR will do the broadest reset for the chip.
Ted – the standard shouldn't mandate the behavior. Should define a default state and that is what to load if you don't know what to do. Making it mandatory isn't the right way.
Carl – wants to do it this way to provide a tool for automation
Ted – feels a default setting will do same thing
Carl – the master reset state is default for TDR.
Ted – what is a "Master Reset" in this case? Ted doesn't have one bit to route to all domains in a chip that would act like a "Master Reset". No master reset pin on chip. Has many reset pins.

Adam C- for each reset domain you want control over, one bit says to look at pin or register and the other bit is the register. 2 bits per domain
CJ – 2 bits per pin minimum.
CJ – from a standards perspective we are leaning towards getting the capability described and getting the end user to have success rather than hoping these things get implemented.
Ted – mandating 2 bits will force designs to get redesigned. Specifying architecture isn't the way to go. Should specify the behavior
KPP – likes what Adam C is saying about the structure of having the 2 bits. Can see the master reset at LSB and more bit pairs mapped higher up the register.
Heiko – concern wants to have something quickly that he can load in that will make sure that the tests are not inhibited by reset register. Something in BSDL to tell what the logic levels should be.
CJ – if it is loaded with all 1's and that is the safe condition.. does that help you?
Heiko – should be a statement in BSDL or PDL that specifies all non reset values.
Adam C – going to have to describe the reset register eventually.
Adam C – if TDI is tied high how do we get the instruction to select instruction if there was an open on TDI. Would scan in all ones and get to bypass instruction and not reset instruction
CJ – would need a bypass escape like clamp hold.
CJ – can we have (clamp) persistence on reset select register independent from implementing clamp release/ hold.
Carl – this issue comes down to whether or not in the 2001 standard, the definition of the TLR state does not interfere with system logic.
CJ – Adam brought up 9.3.1c of standard.
Carl – TLR will remove instruction
Ted – Agrees with Carl that going into the TLR state should not interfere with functional logic.
CJ- The value is in update register not changing. That is what we are blocking
Carl – TRST forces TLR and TLR clears the register. Only need one reset in either case.
Carl – is the purpose of the TLR state to insure that it does not interfere with system logic.
CJ – in general yes but not in this case.
Ted – not including all the other register. There are many other things that have to happen in chips to bring it up other than toggling reset. Thinks we need to apply this concept globally and not just on this single TDR. We should rethink how to control the resets a little and do it globally not locally.
CJ – we have clamp hold that will block everything. And new reset instruction IC RESET. Do we want the designer to add Clamp Persistence to make register survive through a TLR state.
Roland – 2 bits one for enable one for data value. Assuming that it didn't take into account the TRST just the other resets. TRST would still have to negate this register at power up? You can't have a blocking function on the TRST pin
Carl – Correct.
CJ – never ever any blocking on TRST pin.
Carl- should be in rules already but if not will add it.

CJ – when we go into TLR doe these bits clear without having the CPC in place. Do we need to burden the implement of IC reset with the extra rules of the CPC. Could be possible to a bit in a register to see if bits are affected by entering the TLR state.
Adam C- proposes people send out over email Use Cases of resets in and out of chip that will show what sort of solutions that we need.
Carl – may need drop idea of LSB of reset TDR as master reset.

Time has ended and this discussion is moved to email and will continue

Meeting adjourned: 12:03 EST.

Next Meeting: 1/18/2011 11:00 AM EST

NOTES:

Action Item by Carl to elaborate on concerns that he has with OO s on power pins and any rules that would need to be added to the standard to address those concerns.

Current Issues listed and who will champion that issue.

1 Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.

Weekly 1149.1 Meeting coordinates

1. Please join my meeting.
https://www1.gotomeeting.com/join/172495048

United States: +**1 516 453 0012**
Meeting ID: **172-495-048**
Audio PIN: Shown after joining the meeting

2. Other call in numbers
Australia: +61 (0) 8 6365 4094
Canada: +1 416 800 9290
Germany: +49 (0) 898 7806 6462
Netherlands: +31 (0) 208 080 380
Sweden: +46 (0) 852 503 470
United Kingdom: +44 (0) 203 051 4835