Date – 02/15/2011

Attendees: CJ Clark, Bill Tuthill, Brian Turmelle, Carl Barnhart, Dave Dubberke, Craig Stephan, Ken Parker, Roland Latvala, Ted Eaton, Adam Cron, Carol Pyron, Wim Driessen, Heiko Ehrenberg, Francisco Russi, Bill Eklow,

Missing with pre-excuse Adam Ley, Mike Richetti,

Missing: Lee Whetsel, Neil Jacobson, John Braden,

Agenda:

1) Patent Disclosure Slides
2) Update from Editor
    a. Discussion of diff/clean PDF files on web
3) IC_RESET/CLAMP_HOLD Discussion
4) New Business

Meeting Called to order at 11:07 am EST
Minutes:

Review Patent Slide
Discussion of links on PDF from Carl. CJ and Carl discuss how to create links for PDFs. Some members are able to get the links to work correctly in the PDF and others cannot. Carl will look into why this is and generate a new PDF.
Adam C – points out an example of a link that doesn't look right. Line 1519 p36. First rule has no link but subsequent rules do..

Carl Gives updates on latest draft.
Carl asks CJ to give update on BNF and have it run through Intellitech Tools.
CJ will give update.

CJ asks Ken how is feeling about the differences as Ken was concerned about the diffs between today's draft and the 2001 document.
Ken still needs to see the diff. Carl will generate one
Carl will do diff against 2001 document after all changes of the draft are accepted and integrated.. Then it will be a simple diff against the 2001 document.

Francisco brings up the name "Clamp Persistence Controller" of Figure 15-1 and asks if we were going to change it.

Carl moves that we change the name of the Clamp Persistence controller to Test persistence controller
Ken wants to know if should be "Test" or "Test Mode" Persistence controller
Ken Seconds motion.. Agrees we should change the name.

CJ recused himself from the chair to ask questions

CJ – What is the test that is being persisted?
Carl – Ken is correct that it is Test Mode. And is willing to accept the change to the motion

Carl moves that we change the name of the Clamp Persistence controller to Test Mode Persistence controller

CJ – would not be voting in favor of this. Test has many meanings. Clamp persistence and defining what we have persist. IO's are in a defined state defined by the Clamp resistor. Test Mode makes it more value. It isn't a "test mode" that is persistence. And if you have use test modes than it could be confusion. Clamp persistence Controller is more for the novice and clearly indicates what is going on .
Carl- it changes the definition of test logic reset and the definition of Test Mode has been that the IO are controlled by the Boundary Register. So all you are doing is saying that once you are in that test mode you remain in that test mode.. the idea of putting the chip into the Test Mode where the IO are controller and leaving it in that mode is what we are promoting. More than just Clamp.
Roland. Isn't it true you can get into that mode by getting into Clamp?
Carl – we don't want to be bouncing back and forth where the IO's are controlled and not controlled.
CJ- doesn't follow that it is now a Test Mode persistence. Mode we enter with ClampHold and IO are set until we release. Clearly describes as it is with current name.

KPP - sympathetic to CJ's point. Clamp is what is being persistence. But when in EXTEST and have persistence set,
Non invasive instructions behave like Clamp.
Adam C: more definition on Test Mode signal which is what we are monkey-ing with.
CJ – thinks it is fine the way it is.

Dave – since clamp persistence doesn't hold the bypass register and only mode register. Clamp hold implies that it is holding the clamp instruction
Not truly holding instruction if you let the another instruction come in .

Vote. 5 Yes. 3 No 6 Abstained.
Motion Carries.
Test Mode Persistence Controller is now the official name.

KPP – Picture of Persistence Control. Should it change name to Test Mode Persistence Controller. Figure 6-9
Carl agrees that the figure caption needs to be Test Mode.
KPP -Diagram has no Arch for IC-RESET concept
Carl – IC RESET doesn't affect this

KPP – should it?
CJ – no.. doesn't see how
Carl – what should it do?
KPP – could instantiate a Reboot of a system. If that was the case you wouldn't want the pins to be persistence
CJ – covered in prior meeting. Would want to maintain pins in a clamp mode when we have IC RESET. IC RESET purpose to reset on chip logic without having accesss to reset pin. So we can proceed from one test to another . and having ability to keep pins clamped is a win. .wouldn't be in favor in removing clamp hold when we have IC reset
KPP – IC RESET has 2 behaviors. One when clamp is on . and one when clamp is off.
Carl – in descriptive text
CJ – moving towards IC RESET and divorcing from Clamp Reset. IC RESET would work the same way where clamp hold persistence on or off.
Carl – in discussion we point out if system reset function would break the test mode persistence controller of the IO that portion of the IC reset needs to be blocked.
CJ – waiting to see a proposal of the IC Reset. Feels that there are some problems lurking with blocking test logic reset.
KPP – doesn't understand what that means
CJ – right.. We don't have a good understanding of what is controlling the initial state of the TDR.

Ted – if there are 2 ways of doing it why do we pick one over the other.
CJ – Test logic reset,
Ted – we don't need TLR blocking for reset if we have software blocking.
Carl – agrees that we don't need reset hold.

Ted – register must be reset.
Carol – have to define the mechanism of what that is
Ted – going into TLR as other TDRs
Ted – if we don't need it for the other TDRs than you
Carl – Ken ? the largest installed based of test hardware inserts its own resets.

KPP – we develop a suit of tests and each one beings with 5 TMS reset. Also asserts any TRESETS that are available. Normal mode instructions are issued for chain integrity. Then the preparation of test is loaded and then go into EXTEST. Might be 200 elements in Suits. At end go back to TLR and quite. Tests can be run in any order. When the board first powers up it is in a rational mode. And when the first test his EXTEST it lobotomizes the board and IC. When that test completes it does a TLR
Carl – the PDL doesn't have the control over all the TLR states because the tester will use the TLR state as it's parking state.
KPP – would need to make use of new persistence. Would want to set persistence mode at the beginning. And leave it until the end of the test. Next test wouldn't know it was in the persistence state but would in the same way. Sees changes that he would have to implement. Would have to stop hitting TRST. It is being hit absentmindedly. Along with 5 TMS reset.
Carl – can software updates be made for new standard?

KPP – real fly in ointment is every one of these tests starts off with a relay closure. Digital resources are tri-stated during test and relays might be switching around. So you don't necessarily have control of tap port between tests. So each test needs to be "stand alone".

CJ – enter TLR state with 5 clocks of TMS. So what do I gain from discussion.
Carl – cannot guarantee that setting up PDL rules that reset at top level that is not the only time you see TLR. Tester will go through TLR state regardless the PDL says.
Ken's scenario is very different from what CJ and Ted have talked about.
Ted – Ken needs to issue a Test Logic Reset and maintain state.
CJ – Ken , are we achieving what you are looking for in regards to IC RESET?
KPP – yes, I believe so
Ted – what registers do you need to hold state?
Ted – by blocking reset we are changing the 1149.1 state machine.
KPP – for mandated instructions we know what that means. For user defined instructions we are not so clear.
Carl – is it realistic to expect a chip designer to understand No Reset vs. Reset* vs. Blocked Reset or does it create more problems.
Ted – designers today already deal with those scenarios.
CJ – if we don't have a rule than we need a rule. Designer shouldn't be able to take the reset signals
Carl – can't make a rule if it is a black box.

Meeting adjourned: 12:17 EST.

Next Meeting: 2/22/2011 11:00 AM EST

Motion: C**hange the name of the Clamp Persistence controller to Test Mode Persistence controller**
Motion Passed

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Current Issues listed and who will champion that issue.

1 Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8

- Comment #3 Adam L will update language for any proposed change for this section.