Date – 05/1/2012

Attendees: CJ Clark, Adam Ley, Bill Bruce, Bill Eklow,Bill Tuthill, Brian Turmelle, Carl Barnhart, Carol Pyron, Craig Stephan, Dharma Konda, Dave Dubberke, Francisco Russi, Hugh Wallace, Josh Ferry, Ken Parker, Jeff Halnon, John Braden, John Seibold, Peter Elias, Rich Cornejo, Roland Latvala,Sankaran Menon,Wim Driessen,

Missing with pre-excuse:

Missing: Lee Whetsel, Matthias Kamm , Mike Richetti, Neil Jacobson, Ted Cleggett, Brian Erickson, Kent NG ,
Adam Cron , Heiko Ehrenberg, Roger Sowada, Ted Eaton,

Agenda:

1) Patent Slides and Rules of Etiquette
2) Use LiveMeeting "Raised Hand" to be recognized and take the floor
3) System Clocks
4) Register Constraints
5)

Meeting Called to order at 10:38 am EST

Minutes:
Review Patent Slide – Slide Presented to the Group.
Solicited input from anybody who is aware of patents that might read on our standard.
No responses

Review of Working Group Meeting Guidelines
No Objections

INIT-SETUP
Dave – all parts have to power up at some time. When they came up they are in mission mode.
Ken – init setup instruction would be done in devices that had it and the other devices that don't have would be doing something non invasive. Those that had init-run, that was felt to be invasive and would pass control to boundary scan. Those without init run would go to EXTEST.
Ken – are you viewing init-run as non invasive?
Dave – has changed an electrical parameter. No difference from powering on.
Ken – also envision init-run doing other tunings like turning off PLLs. That seems invasive.
Dave – it is invasive internally. But not externally to the IO pins to itself. Thought this was an issue of a chip damaging other parts on the board.

Ken – there is the damage issue. But there is an issue with the board running amuck. See that as a concern. If there is an undetermined amount of time where parts respond. Trying to minimize that window of time
Dave – key point is that the part has to come up from an off state. And it is not in a test state.
CJ – not going to just turning off PLL's in init-setup.
When the chip comes up we are getting it into Mission mode or the IO is off.
Concerned about ability of test engineer to synchronize all of the parts coming up.
FPGAs are in a tristate state when it powers up if it is not programmed
Would like other parts to act like that.
Remove the burden for the test engineer is to have the outputs off.
Carl – init-setup and init-run were modeled after pre-load and EXTEST. Starting to try and tweak that might be a significant amount of work.
CJ – might be the model but might be a mistake. Hate to go into ballot with a mistake.
Ken – would like some input from the IC vendors on the call.
CJ – would like to relax the rules when saying you can have any change in the IO while in mission mode.
Ken – what are the other IC's doing that don't have that instruction.
CJ – nothing which is useful. You would haven't have to do anything with those IC. If the chip didn't have init-setup than it would just go into EXTEST.
Roland – Need some time when IO's are turned on. Concerned here if we go into a tristate behavior how much time do we need to have before we can use the IO.
CJ – rules as written in preload you would enable control cell. You would still have that amount of time in a scan operation.
Rolland – model here was to use init-run to setup pins.
CJ – at least allow the pins to go into EXTEST
Dave – reason we were pushing this is that we have to wait also.
Not really understand why we need to have tristate ability when these interfaces are typically unidirectional.
Just need to manage the one that is programmable.
Most cases these IOs are off to start with.
What is the mechanism to tell it to go .
CJ – currently it is EXTEST or init-run
Dave – in mission mode ?
CJ – according to the rules right now you can do that. Nothing should be changing.
Dave – parts come up when power is applied.
Carl- the rule is that JTAG test mode can't do anything to the part. Not Mission Mode
Ken - Init-setup was originally going to be one by one setting up the parts.
Significant amount of time between the first part and last part hitting EXTEST.
Safety issue might not be chip to chip but system wide
Preload across system
Concerned with different views of init-setup we could introduce extended amounts of time between some parts setup and others that are not and you get strange things happening.
CJ – need to get more concrete on strange things.

Not seeing the issue of having one chip programmed and others not programmed at the same time.

This is why the example shown has the unprogrammed parts IO are tristate.

Rule might be overly strict.

Ken – could have situation where pin to DC/DC converter would be tristated and you wouldn't know what the dc/dc converter does.
CJ – board designer would take care of that.
(referring to CJ's slide Required INIT_DATA Control)
Carol – requiring 2 control cells for the same IO.
CJ – when we change the parameter the output is not being affected.
Carl – not two control cells. This is a form of High-Z
Carol – high z for the entire chip.
CJ – every bit.
Carol – than it would be 2 control cells for the same IO
CJ – it could be shared.
CJ – what this proposal is saying
Carol – you don't have to be in system mode to program your IO settings.

Feels it's over kill

CJ – init-setup the chip is in mission mode.
Carol – you don't have to use have to use mission flip flops to program IO. Not in test mode. But you may not have locked your PLLs. Or doing any functional actions. Might have just powered up and wiggling temp pins.
You are pushing the model that you are using the mission mode flip flops as test flip flops.
CJ – not in the slide.
Carol – define characterization
CJ – system level test engineer, I have a chip on the board and would like to take a look at the eye diagram of the SERDES chip to chip. Characterize your design to make sure that the board works as designed. In that mode you would want to control the SERDES to be able to analyze the signal quality.
Carol – finding the best differential swing for the SERDES is a dynamic process. Not just set a setting and use it.
Carol – SERDES BIST is different than init-setup testing for defecting.
CJ – point was that the system designer would like to adjust the differential swing during his testing process.

Carl – if you are talking about init-data being per IO to control each IO independently, as a previous chip designer I would protest. Already that mechanism in 2001. Need to make init-data an invasive instruction and use PreLoad. Adding this much complexity to the init-data does not give me any control beyond using software.
Init-data as an invasive instruction would end these discussions.
Use PRELOAD

CJ – will take another stab at it using PRELOAD. Don't need to say init-setup is invasive.
Carl – just saying the boundary register is now in control of the IO.

CJ – don't seeing the boundary register taking a rule in init-setup.
Carl – don't care if it is the boundary register. HighZ is an invasive instruction.
Make INIT-DATA invasive and require a PRELOAD before it.
Carl – will concur that the scheduling of init-setup and init-run is creating problems.
Making init-setup an invasive instruction, it takes control, is the simpler setup. You can eliminate all the requirements.

Hugh – let's not confuse characterization with time constrained when running boundary scan. What we are doing is mixing up characterization and what we are doing with instruments. But don't want to break what the manufacturing guys are doing. Just need basic tools and instructions without mandating bits.
CJ – was to avoid making additional instructions that are different than what the other board test engineer use.
Ken – expresses sympathy that init-setup might become a test instruction. Would go into init-setup with some setting for the IOs. And then go in and mess around with voltage levels on the IOs. Assuming the IC people are comfortable with voltages changing on the IOS while in a frozen state.
Carol – if we are going to make init-setup intrusive it should be as if the IO is applied. Not do anything in the way of capture dr.
Ken – might be important on a small piece where you need a stable state on some pins. Wouldn't want the whole board go into high z in lockstep.

Dave - was proposing not to use the boundary register for init setup and init run. Trying to address how the io gets electrically configured prior to EXTEST. Primarily voltage swing. Get setup with init setup init run and then do preload and EXTEST.
CJ – would it be a problem to do preload and then the settings.
Dave – no. Whatever you have to do to get your board up and running .
It's getting it ready electrically. Either mission mode or other time.

Roland – loosing perspective on init-setup and init-run.
Why can't we use init-run for all these scenarios
Carl – big difference between init-data and init-status registers is that init-data can be very long. Wanted to restrict to accessing init-data only once.
If we stay with preload EXTEST model we should move things to init-run. And try and keep the long init-data to minimum number of scans as possible.

Ken – if init-data has cells in it that turn on sections of the boundary register. Than the preload and init-run setup might put the boundary register in the wrong state. Segmentation bits might need to be in boundary register.

Discussion to continue on the Reflector.

Meeting adjourned: 12:04pm EST.

Summary of Motions Voted on
0 Motions voted on

Next Meeting: 5/8/2012 11:00 AM EST

NOTES:

1149.1 working group website - http://grouper.ieee.org/groups/1149/1/

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Meeting time: Tuesdays 10:30 AM (EST) (Recurring)

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