

1149.1 Working Group Meeting Minutes. December 1, 2009

Attendees :

Ted Eaton
Roland Latvala
Wim Driessen
Ken Parker
Bill Tuthill
CJ Clark
Dave Dubberke
Carol Pyron
Francisco Russi
Adam Ley

Agenda:

- Old Business
 - a. Heiko's proposal of adding Power/Gnd identification
 - b. Francisco's proposal on adding NC to pinmap
 - c. Report from INIT group
- New Business

Meeting Called to order at 11:02am EST

1. Old Business

- a. Heiko's proposal for adding Power/Ground identification
 - CJ – can we do this in the port and have it be NON-VHDL
proposed using Power_1, Power_0, Out_linkage, In_linkage
 - Ken – if we add new things to language they should be optional syntax so that it doesn't break everyone's tools. Maybe do this as a BSDL extension.
Change the conformance statement to break tools in a graceful way. New syntax could be added in quoted strings so BSDL parsers can still read BSDL file.
 - Carol – Continue to call power pins linkage and add section later to add properties to linkage pins
 - CJ – does not want to do Extensions. If it isn't in port statement it could be left out and not get acceptance to incorporate this.
Improves diagnostics
 - Ken - BSDL extensions allow you to define new attribute. Typically found at the end of file. All tools will skip extensions
 - Francisco – could we use design warnings
 - Ken – design warnings have no syntax. Only used for comments.
 - CJ - we should focus on either additional types in port section or use as Extensions.
 - Ken – Extensions would be allow this to be added without breaking tools that do not want to support this.

Adam – it would be useful to understand why we are trying to add these types and its usefulness.

Changing the port statement would be a complex change.

Liberalize the rules of the BSDL extensions and allow them to be somewhere other than the end of the BSDL

CJ – feels that changing the location of BSDL extensions may be more difficult than adding new ports

CJ – Don't know what the pins are. Linkage groups all pins into a category of non boundary scan. Allowing these different types would allow for the tools to know that pins are power/ground pins. This will give the tools more information for diagnostics to know if pins are power/grounds. Benefits to know which pins are connected to different power rails. Will give ATPG more information if directionality is knowing for pin and enhance fault coverage.

AI - CJ will capture this concept in text to give the group something written to review and decide upon.

Ken – should have a short prioritized list of topics that we are working on for the working group. How do we develop this list and keep the discussion short.

CJ – We currently do have a short list. Main priority is to manage observe only. Other items need to be taken on. There are approximately 5 things to work on. INIT is being worked on Tiger Team. These items were discussed at ITC.

Ken – May want to add thresholds on receivers to list (JJ's topic of discussion)

Dave – JJ is working on proposal to give to WG

CJ – in favor to add attribute to add resistance to driver to show if coverage is available.

Ken – show the designer(guidance) how to properly design cell to allow the receiver to correctly detect the signal. No guidance given today.

Ted – would like to have a description of what we are working on.

CJ – we can add topics to the website

Carol – designate power/grounds/nc/reserved as linkage pins. Plus multiple package options so some pins become internal. When defined as linkage it takes it out of boundary scan complete. Don't expect boundary scan tools to do anything to those linkage pins.

CJ - on an FPGA you can have a pin that is defined as a linkage pin but might have a signal connected to that pin and may need to toggle and would like to know if it is an input or output so that you can either driver or not drive that pin.

Carol – worried someone will use the out_linkage or in_linkage to get around being non compliant.

Ken – are these only hand crafted tests on analog pins?

Ted – If BC7 cell is connected to this linkage pin than this could be used to check for shorts not necessarily to an analog test.

Ken – sees this example as a good reason for adding this capability.

Need list/examples of advantages/scenarios for using this.

Wim – Can the input pin withstand the voltage when driving? Maybe more information is needed than just input/output

Adam – need proposal

Francisco – add in / out linkage. Currently a lot of work to know directionality of the pin

Ken – system he works in has BSDL description but that is only for boundary cells. Knows voltages / analog pins from another file (setup library)

Bill – tool vendors don't get the setup library.. Generally only get the BSDL file from Chip vendors. Having this information would allow better coverage. Linkage is a catch all.

Ken – IC industry has spotty record and usually does not generate accurate BSDL. This may cause problems

Adam – how do Setup Libraries get created?

Ken – semi automatically at best. But some are created by hand.

Setup library prototypes get created from BSDL

Ken – possibly a simple BSDL and advanced BSDL

Ted – IC vendor can use “linkage” if they don't want to add extra information.

Ken – consumer could hand edit the BSDL to add in /out to linkage

Francisco – this is a question of what are true linkage and not true linkage

AI – TED will draw up some examples of how this would increase short coverage

b. Francisco's proposal on adding NC to pinmap

AI - Francisco will draw up some examples of No Connect

Carol – worry about case of pins going from 1023 pins to 768 pins

Have different ID codes for different packages

If it is all in one BSDL how does the customer know which package to use when they get the ID code back.

CJ – user will have the netlist of the board which will show the package that is being used.

Ken - the only variation of no connect is used for linkage and not for I/O pins.

c. Review of INIT Tiger Team

Carol – INIT – examples of side files were discussed.

Carl sent out minutes of Tiger Team

Meeting adjourned at 12:15

Next Meeting: Tuesday, December 8, 2009 11:00 am EST

Action Items:

- Ted will draw up examples showing a BC-7 cell connected to a linkage pin and how it would improve shorts coverage
- Francisco will provide examples showing the use of NC over different packages with the same die.
- CJ will draft a list of topics this Working Group will cover so that the group will have it to refer to. This list will be added to website.
- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- CJ will make changes to draft for observe only
- CJ will Add a figure and little text to address TRST use with interconnection of components
- Adam to add comment about TRST. Update figure 6.8
- Adam will update language for any proposed change for section 4.6.1 that deal with the polarity of TRST.