

1149.1 Working Group Meeting Minutes. January 12th, 2010

Attendees:

CJ Clark
Bill Tuthill
Dave Dubberke
Ken Parker
Carl Barnhart
Adam Cron
Carol Pyron
Wim Driessen
Francisco Russi

Agenda:

Review task status

Minutes:

Meeting Called to order at 11:05am EST

Update of Task List.

CJ started proposal for changes that he needed to make.

Added LINKAGE_IN / LINKAGE_OUT / NC / POWER_0 / POWER_1 to reserved words of BSDL

Carol – NC is common pin name. is this an issue? Having a key word of NC reserved.

CJ - NC is in pin map not in port.

CJ – Pin type added as well. Linkage_in /linkage_out/ power_o /power_1

Francisco – NC is a linkage in the package.

CJ – still leave linkage available so that you could continue to write BSDL the old way. If you want to add more detail then you can use the new keywords.

Carl – if power0/power_1 are optional than can't remove power and ground from definition of linkage.

CJ – power0/power1 is to identify the pins that are connected to power rails versus of analog inputs.

Carl – Power0 is also ground

CJ – what we are trying to doing is identify what pins are power rails.

More dealing with different voltages on the board and difficult to identify those voltages automatically.

Carol – might want a linkage_power and not assign a level to it

CJ – want to identify the difference of power rails for pull up and pull downs.

Want to identify resistors that are pull ups and pull downs.

Carl – would have like to see power_gnd or power for clarity

Carol – linkage_power linkage_gnd instead of the Power_1/ Power_0

Ken – want to keep the VHDL (IEEE 1076)standard syntax in the BSDL

CJ – what is the gain to have the port statement map to VHDL?

Ken- decision was made long ago and BSDL was advertised as a subset of VHDL. Possible people are relying on ports being VHDL syntax and could cause a tool problem if non standard VHDL syntax is added to port statement. Could also be a don't care if no one cares that the port is VHDL syntax.

CJ – Not aware of tools that use BSDL and VHDL the same way. No simulator out there that supports BSDL. Concerned about small if any part of industry.

Ken – tool built on VHDL assumptions could exist. Need to understand risk versus gain. Doesn't see gain

Carl – since it has been advertised as VHDL for 16 may be people on ballot that would object to undoing that. Maybe only risk to get it approved.

CJ – willing to take risk and if doesn't pass than that would be good feedback.

More marketing fluff than anything that helps the industry.

Many differences in BSDL than VHDL. A VHDL compiler could not consume it. No need to keep BSDL a subset of VHDL.

CJ – most people parsing BSDL would be able to update their parsers to take in the new syntax.

Carol – likes the attribute idea. has internal tools that would have to change more than necessary.

Ken – if we change the VHDL syntax than we would have to divorce ourselves from the VHDL standard. Why take risk. Might want to ask some of the people who were involved in the original decisions. VHDL thing is sort of a crock. But that is what the IEEE wanted.

Ken – 3rd question. . why would I learn something about a system node. (example ground plane) why do I need to read BSDL to learn that a certain pin of a device is tied to ground plane. Why not tag it as ground. Attached to ground on board..

CJ – this is for some of the more complex parts available today. (example USB port labeled as linkage. Voltage pins have no definition) separate grounds for oscillators.

Ken – only a few unique nodes that these pins are connected. Possibly all tied together.

CJ – not all tied together.

Ken – Grounds are all at same potential.

Ken – define analog pins and in/out and leave out of boundary scan register because they are not digital.

Carl – tool is still going to be changed if in/out is defined and not in boundary scan reg.

Ken – tools see that today and generate warning that pin isn't in boundary scan register.

CJ – loose some checking with that because you don't know what the designer had intended.

Carol – differential pins should being boundary register. 1149.1 makes provisions for differential pairs.

CJ – allow you to exclude a pin that is analog. Provides a loop hole where you can leave these pins out.

Carol – likes Ken's idea to call these pins in/out and leave them out of boundary register. Provide a note that says that they were left out.

Ken – people design chips leaves these pins out of boundary scan and they have 2 choices – document direction of pins. Or they can use linkage to hide it. In the end when you try and test the part on your board there is a loss of coverage.

Carl – who raised this issue and why is it a problem. What is the definition of the pin. On a analog pin knowing if it is driving could be useful. But on the power why is it important to know.

CJ- you know which way the pin is pulled. Netlists don't easily show you what the signals are.

Ken – the generic netlist may not have the nature of those particular nodes. Doesn't show what the power/ground of the pin.

Carl- by the time you get to test the proper place for the power information is the board netlist not the BSDL.

CJ – with all the different powers that are available , the target audience is not available in identifying this. A lot of people miss the power rails. Knowing where those power rails makes the board test job a little easier.

Carol- should make the change but not should be port list

CJ – easy to add into parser if in port statement.

Francisco – expanding the section comment section. Force comments on BSDL. Doesn't want to unlink from VHDL standard.

Adam C – BSDL have some package information to tell tool about power/ground

How is a pin power and ground?

Carol – power pins may be power or ground based on power down mode of chip. If you are not using it can be 0 volts.

Should always have linkage option.

Wim – Rely mostly on naming convention in netlist and not from component. Linkage in and linkage out will help. Wonder where is advantage if you know if the pin is power or ground

CJ – there isn't a clear way to know what the power pins are from the netlist at least in an automatic way. Becomes a manual effort to identify different power pins

CJ – should have a vote?

Wim – not strong position one way or another. Would be helpful and not that bad of a change. Wim does not use VHDL for their parser.

Carol –idea would be better as a second attribute.

Carl – would also cause the checking to know it is not in the boundary scan register and that would be ok.

Carl – would put forward a motion to add attribute that would identify pins that are in port list that are in/out/power/ground

CJ – Would rather scrap everything and motivation would be to change just what is needed for .6 and abandon everything else.

Best to make the small change for the .6 need and incorporate the INIT change if there is time. Not getting anywhere with the other issues.

Carol – these are normal engineering discussions to make a better standard and not place an unnecessary burden upon everyone

CJ – Working Group is not making progress fast enough. Would rather do one small thing and get it done and move on

CJ – next week CJ is tied up. Move to cancel next meeting.

Carl – one more meeting to make sure we are not dropping and anything that needs to be done.

Carol – agrees.

CJ – Heiko had initially brought up the power and grounds rails being added to the port list.. Indication that other people besides CJ wants to have these things done.

CJ – Next meeting will be on the 26th.

Meeting adjourned at 12:16 EST.

Next Meeting: Tuesday, Jan 26 11:00 am EST

Current Issues listed and who will champion that issue.

- 1 Observe only. – Ken
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale)
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – CJ and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.