1149.1 Working Group Meeting Minutes. February 2nd , 2010 v2

Attendees: CJ Clark, Bill Tuthill, Dave Dubberke, Heiko Ehrenberg, Ken Parker, Adam Cron, Adam Ley, Roland Latvala, Carol Pyron, Wim Driessen, Francisco Russi,

Missing with pre-excuse: Carl Barnhart

Agenda:

11:00AM

1) Adam Ley – TRST

11:15AM

2) Ken -- OO on I/O pins

11:30AM

3) Carol - Constant Values for Sample

11:45AM

4) CJ - Review of TRST submitted figures

11:55AM

5) New Business (if any)

Minutes:

Meeting Called to order at 11:04 am EST

Review of individual tasks

Discussion of the TRST rule update – Adam L

Review of Adam L's TRST rule update – Walk through email that Adam sent. Email attached at end of minutes

May not be "relaxation" just more of a change.

Adam L was guided by comments mad by Doug Way

4.6.1.C – TRST should be clarified to not affect functional logic in any way

Carol – TRST doesn't affect system logic in her chips. Toggling TRST will take JTAG out of the way so that mission mode resets can take affect.

Adam – TRST should not be held low to obtain functional logic.

Ken - Parts binned in test mode and then assert TRST, system logic is affected by pin stimulus while in test mode.

Adam L – system logic can not be affected by change of state of TRST.

Adam l – affect is not limited by TRST. Normal mode instruction could have affects on chip after test. This rule change doesn't intend to address that at all.

CJ – more an artifact of being in Test Logic Reset and not by the TRST pin

Adam L – There few dozen places where TRST needs to change in the draft. Change needed everywhere there is a TRST *. Changes spread through out sections 4 and 6

Adam L and CJ will work together to get changes in to draft. CJ will change the draft where he knows it needs it and give to Adam to review.

CJ – doesn't want to change TRST * to TRST-pull down everywhere. Wanted to relax rule on pull down.

CJ – don't want two different chips with different sense of TRST. This could cause a problem at the board level

Adam l – compliant chips have pull ups now.

Ken – does not have information read for a discussion on Observe Only and is willing to give up his 15 minutes to allow this discussion to go on regarding the best way to change the draft for Adam L's TRST change.

CJ – make more sense to cover the technical material rather than the mechanics of a draft change

CJ – Need the Observe only change more than the TRST change. Observe Only is a high priority.

Ken - will try to have information ready for next Tuesday. Needs to collaborate with Carl B.

Carol- OO is a good change to make over all.

Ken – returning to mechanics of changes. Concerned that the groups working in parallel may make a difficult job when trying to put the pieces together in the draft.

CJ – concerned is noted. But doesn't see it as a problem and can manage the integration of the different pieces.

Constant Value for Sample – Roland/Carol

Carol was not able to get to change the text

Carol –easiest way to make changes is to update tables and review with CJ on the side. Will try and make changes for next meeting

Discussion now turns to CJ's submitted change for the TRST figures.

CJ – figure not final. May need different wording.

Adam L – figure 4-4 TRST label inside the chips need the *

If we add TRST PD * need a diagram to illustrate that as well.

Adam l – figure 4-5 addition notes may be helpful. To separate board level VS chip level

CJ – has two figures with caption that reads "inside the IC". Figures made but not currently in document.

Adam L – 3 segments should have labels A,B,C for easier reference

CJ – already has this in more recent version

Adam L – Diagram A (pull down) should emphasize that node is for connection to Bus Master, and Diagram B TRST * node is NOT for connection to the bus master.

Ken – two other cases to talk about? Chip with TRST that is NC and Chip with TRST that is tied high to logic 1 with no access. 2 cases of inaccessible TRSTs

Adam L – Not Valid!! Has to be board level conditioning to TRST.

Ken – TRST has internal Pull up to Logic 1 with no access to it.

Adam L – Not Valid.

Adam L – not valid by the way TRST is defined. Has to be strobe on power up

Adam L – synchronizing sequence is only valid if TCK is wired and strobe.

Adam C – has to power up immediately.

Adam L – TRST Has to be properly conditioned at board level

Ken – Like to see added parts D and E of drawing are to show the wrong ways to hook up TRST

CJ – separate figure for how not to do it should not be in this section.

Francisco – TRST with Pull up seems to be ok, up to designer to take the risk. Should make some recommendations with regards to this scenario

Adam L- designer willing to take that risk should be shot.

Ken – it may be worth a quick picture to say that this layout is deprecated.

Ken – Ken's case of No connect is at board level. Floating lead. The pad is soldered down but there is no signal at the TRST pad.

CJ – this is why we are showing A,B,C. This is how we manage connecting TRST.

Ken – maybe add some words to say you CAN'T connect a TRST in this way

Adam C – Motion – add another diagram to the TRST figure showing bad behavior . These would be used to show the user how to not connect TRST.

Dave – pin coming out with internal pullup is that valid.

Adam L – no it is not valid.

Dave - POR internal why is not valid.

Adam L – if documented with POR it would be acceptable.

Francisco – add to BSDL when no TRST is connected.

Adam L – missing the point has to do with internal POR and no TRST.

CJ – when TRST is present in BSDL, this tells tools that it must toggle or hold low to initialize tap controller. In order to achieve something whre you could leave TRST* unconnected at the board level, we would need to add language to the BSDL to tell tools that TRST* is there but that the tap controller is reset at power up by an internal POR.

Francisco – 2 other things mentioned on power up reset generator. Also put in BSDL a way to capture the time that takes to trigger the reset.

Carol – that should not be in the BSDL. BSDL has very little in the way of timing information. Should know in terms of 1 tck cycle.

Francisco – longer than 1 tck

Adam L – how long does it take for reset to be released. Would be extraneous information.

CJ – have to wait for other things on the board to wait for than just the POR. Need to wait for other devices to power up. More of a novice problem.

Rolland – when chip has own internal pull up and is there any specified size resistance

CJ – no, the logic family for the TAP is not defined by the standard so there is no recommended value to use for an internal resistor

Rolland – if there is an internal pull up might need a recommended external pull down size.

CJ – no way in standard to specify what it should be because we don't know what will be on the board and how many devices connected.

Adam L – TRST is actively buffered should also be illustrated.

CJ – should we show buffered TCK as well?

Adam L – where appropriate buffering should be recommended.

May have TRST on 20 chips. May have to put 10 ohm resistor to pull down trst to 0

CJ – Partitioning would be a method.

Adam L – Figure A is raising some electrical issues that should be address. Seems to preclude the adoption of a buffer because the TRST illustrate appears to be the same as illustrated in 4-4. May want to also show a diagram using a buffer on TRST.

CJ – After 12:00 Adam C's motion to add "bad behavior" figure for TRST will wait til next week.

Also remembered that we did not vote on the syntax for No Connects. Will make these 2 votes the first order of business at next meeting.

Carol – wanted to note that CJ's changes to the wording for TRST looked good.

Meeting adjourned at 12:06 EST.
Next Meeting: February 9th 2010 11:00am EST

Next meeting first order of Business will be to take care of our 2 motions that have been made.

Ken's No Connect proposal and the also vote on adding the "what not to do" figures

Adam C motion to add to the spec some 'what not to do" diagrams for the TRST* figure that CJ is changing. (paraphrasing as a formal motion was not made)

Current Issues listed and who will champion that issue.

1 Observe only. – Ken
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale)
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – CJ and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.

Adam's Email set on 2/1/2010 regarding the updated rules for TRST*

Title

(a succinct name for the item)

- Update rules for TRST*

Who

(originator/ lead proponent)

- Adam W Ley
  (NOTE: much of the impetus for this item is based on reaffirmation ballot comments submitted by Doug Way)

What

(what problem is seen, what remediation is sought)

- Consider that rule 4.6.1 c) needs to more fully restrict the use of TRST*.
- Consider illustrating the use of "card-level" POR for TRST*. Consider also illustrating of other means of treating TRST*.
- Address the concern about use of the term "hard-wiring".
- Consider also specification of "nTRST_PD" as defined by 1149.7.
- Consider also need to modify language in 6.2.1 a) and elsewhere that implies *transition* on TRST*.
- Ensure uniform and appropriate treatment of TRST* throughout the document.

Why

(why action is sought, to what/ whose benefit)

- There is still much confusion about the appropriate use of TRST*.
- Per reaffirmation ballot comment # 3 against subclause 4.6.1, as submitted by Doug Way, "Datasheets for some devices imply that TRST* needs to be low for normal operation. In many cases this is not accurate."
  Proposed Change: 4.6.1 rule c) TRST* shall not be used to initialize or effect the operation of the system logic within the component.
- Per reaffirmation ballot comment # 4 against subclause 4.6.2, as submitted by Doug Way, "Add comment that TRST* may normally be driven from power-on-reset on the card to initialize the test logic within the component."
- In general, TRST* should NOT be hard-wired – rather, if it is desired to be "strapped" low for normal system operation, this should be done by way of a pull-down resistor and the signal brought out to a testpoint/ header pin for connection to an external test if/ as may be required.
- Per IEEE 1149.7, a new sense of TRST*, therein called nTRST_PD, has been defined. It behaves identically to TRST* (nTRST) except that it is conditioned such that an open circuit presents a pull-down effect; this is desired (required) for fail-safe operation in some safety critical applications.
- At 6.2.1 a), use of "transition" might be taken, mistakenly, to imply an edge-sensitive characteristic for TRST*.
- At 6.3, the rules/ discussion will need to be harmonized with these other changes.

How

(how would the problem be addressed, how would the solution meet the desired remediation)

- Restate rule 4.6.1 c) to clarify that its assertion (or lack thereof) can have no effect on the system logic.
- Add text and diagram to describe and illustrate use of “card-level” POR for TRST*. Add text and diagram to illustrate other means of treating TRST*. Ensure that it is well communicated that the ONLY appropriate use of TRST* is to ensure that the chip TAP powers-up into its Test-Logic-Reset state (optionally, TRST* can be tied low indefinitely to ensure that the TAP remains at TLR).
- At 4.6.2, paragraph 3, replace “hard-wiring TRST* to logic 0” with “wiring TRST* through a pull-down resistor to logic 0”.
  (NOTE: CJ has already incorporated this into the draft in work as of 2010 Feb 1)
- Add TRST_PD* as a peer-wise alternative to TRST*. (NOTE: this will touch many points throughout the text)
- At 6.2.1 a), replace “transition” with “change”; add “NOTE – This rule does not intend to suggest that TRST* has any sort of edge-sensitive characteristic; rather, per 4.6, TRST* is strictly limited to a level-sensitive characteristic.”
- Changes for 6.3 require further analysis/ review pending completion of these other changes.