1149.1 Working Group Meeting Minutes. February 16th, 2010

Attendees: CJ Clark, Bill Tuthill, Ken Parker, Dave Dubberke, Roland Latvala, Bill Eklow, Wim Driessen, Heiko Ehrenberg, Francisco Russi, Adam Cron,

Missing with pre-excuse: Adam Ley, Carol Pyron,
Missing: Carl Barnhart

Agenda:
Review init
Review power and ground
Feedback on drafts sent out to working group

Minutes:
Trouble with GOTO Meeting
GOTO Meeting finally is underway at 11:27am

Review of changes made to draft.
CJ asks for feedback and none is given

Latest draft on website. Draft has change lines where it differs from 2001 version.
Added figure 11-10. All figures after that are different and cross references are different
CJ- Push back from Carl and Carol on recommendation vs permission on OO.
CJ – Sees this as a recommendation from a Test point of view.
Carl and CJ traded emails over the past few days to discuss this. One idea is to remove SAMPLE from being required on OO. This would make OO easier for designer to implement.. Figure 11.10 shows the conceptual schematic of OO on differential pairs.
CJ -With LVDS the tools can't detect certain class of faults even though mission mode (single mode side) is showing a 1 or 0. Diff receiver can work ok at slow speed as there is still enough current to the receiver to trigger a 1 or a 0.. At system speed functionality however you would detect a fault such as a short to ground on pin.
Given the shorten time we will address the comments next week.
Ken did not see the changes that CJ had made when looking at the draft on the ieee website. The draft on the website was checked and did contain the changes.
Action Item is to look at draft and go over comments for Observe Only section
New Draft on Website. Under current draft link
http://grouper.ieee.org/groups/1149/1
CJ needs some text to go with latest PDFs that were sent out.

INIT discussion
Init section – What differs here are TDO_MNEMONIC & TDI_MNEMONIC for init instructions. This is a useful way to allow designer to set up init instructions.
Ken – don't need TDO or MASK on data going in for INIT. When we are loading into INIT SETUP it is IN going only..
CJ – how about status during the write?

Ken - different register and status. STATUS is its own instruction register.

Init run may target status register but doesn't need to

Status register is output only.. No TDI but could have TDO and mask.

CJ – don't see why we wouldn't want to include TDO and MASK when necessary

Power and Grounds

CJ presented a power point on the need for adding linkage Power and Grounds to BSDL

Model the components. All non boundary scan components need to be modeled so understand what the parts are driving and where power and ground pins are. If you don't know what the pin is doing you make it a linkage. Makes limitations on tools because it doesn't know how to use the linkage pin.

Modeling difficulty has increased due to complexity of trace through and as new devices are introduced.

Algorithms used to divine the power and ground pins. Doesn't work all the time. Many power and grounds being used today.. Bigger job than it used to be. New need to understand the relationships between power and grounds with things such as PLL, SERDES, DDR, etc

Trying to add information so the tools can make heads or tails of the topology that is present.

On linkage identify in and out and also have the ability to call it power and ground as well.

Power 0 and Power 1 are not to do with logic levels but that it has a power or ground connected to it. Only looking at the Digital value 1 or 0.

This will help give better diagnostics and fault coverage.

Link power to pins we can identify the power pin if there is a problem on a signal pin that is associated with a specific power.

Ken – 3.3 volt pin blindly assume that is a 1. No information from cell what 3.3v is interpreted as.

CJ – If 3.3 is pull up on boundary scan cell than it is most likely used as a 1. Assuming that designers are doing things that make sense.

Ken – making assumptions will make tests not pass on good boards and will need to be debugged.

Ken – can't make assumptions that can be occasionally wrong.

Ken – if 3.3v goes to 2nd IC, different vendor,

Bill – linkage power 1 and power 0 can be used for pull ups and pull downs and linkage can still be used for obscure cases. If the designer feels that the pin should not be considered a "power1 or power0" it can still be labeled as a linkage and ignored.

Ken – input buffer has threshold. We don't know what the threshold is. If we connect through a resistor or defect how does it get viewed, as a 1 or 0?

CJ – Would like to add thresholds to BSDLs but if we can't get past this it might be too much to get into adding thresholds.

Ken – Would like to do a full robust change.. Not one that might be prone to errors

CJ – not getting coverage that we need. This would help increase the coverage.

Heiko – Agree that threshold would be important to know. Would like to make it part of the BSDL.

Roland – would you classify the power 1 as a certain voltage (ex. power 1_3.3 , power 1_2.5)
CJ – current proposal is for just Power 1 and Power 0 with no differentiation.
Roland – all powers then would look the same no matter what voltage is applied
CJ – would like to indicate the voltage thresholds but we're not ready to go that far.
CJ – still gathering information
Roland – what if you had 3.3 shorted to 2.5. This could burn something up.
CJ – that is more of a power off test. Not in the 1149 domain
Roland – BSDL not differentiating the power levels. This is something that is important.
CJ we are trying to get the agreement that this is the direction that we need to go it.
CJ – Ken and Neil Jacobson did presentation on grouping power pins with signal pins.
CJ – This will allow us to back into a problem
Ken – 2008 ITC paper that he put out and example BSDL
CJ – should we put the paper on Website.
Ken – put it in the private area. Pass it on to Adam and to put it in private area.
Ken – no doubt that linkage is a problem. Linkage is a black hole that we hide a lot of useful information in.
Roland – internal pull down on cell you would get voltage divider not pull for analog purpose.
CJ – would be good to go after 99% of problem and put something in standard to help address this rather than avoid it because of a 1% issue.

Meeting adjourned at 12:17EST.

Action item for everyone – take a look at changes (text and figures) to draft and see if there are any concerns. New Draft on Website. Under current draft link
http://grouper.ieee.org/groups/1149/1

Next Meeting: February 23th 2010 11:00am EST

Current Issues listed and who will champion that issue.

1 Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. "No Connect" – Ken and Francisco.

8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments
- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.