

1149.1 Working Group Meeting Minutes. March 3rd , 2010

Attendees: CJ Clark, Bill Tuthill, Adam Ley, Carol Pyron, Adam Cron, Dave Dubberke, Roland Latvala, Wim Driessen, Francisco Russi, Ken Parker

Missing with pre-excuse:

Missing: Bill Eklow, Heiko Ehrenberg, Carl Barnhart,

Agenda:

11:00 Summarize action items taken on feedback received.

11:15 Wrap up of linkage_in/linkage_out

11:30 Power-up/Power-down wrap up?

11:45 Open discussion/New Business

Minutes:

CJ has taken all email feedback for draft and incorporated feedback into the draft.

Observe Only.

Carol. Put OO on pins successfully without checkers complaining

CJ has some ideas for different OO designs.

CJ – Relax rules on redundant OO cells

Adam L– if you want to identify redundant cells and liberalize the rules for the cells it needs to be done more expressly.

CJ – Cell design at transistor level is easier if you aren't required to have SAMPLE there. Original standard had BC_4 and function input.

CJ – BC_4_observe only came much later. Why did we need that?

Adam L– reason to have it was to distinguish the cells with the OO function from the cells with a controlling function. Input cell associated with port and additional (redundant) cells that also are associated with port. Only one of those per the rules of DOT1 can have control function. OO is necessary to indicate those cells that do not have control function from the one that does. Does not in anyway free them from the other rules.

CJ- this is the case as currently written

CJ – OO is not always the redundant cell, it takes the place of output of differential receiver would be traditionally BC_4 function. This Breaks ability to remove SAMPLE.

Ken – what does remove SAMPL mean?

CJ – SAMPLE on OO would not function. Would be like not having INTEST.

Carol – per pin?

CJ – Yes per pin. SAMPLE instruction would still be required on inputs and outputs. But redundant cells would not be required to have SAMPLE. This may make it easier to implement.

Adam L- Remove Sample – Capture value of Sample would not be required to be PI but could be X. the OO function would apply in logical sense only during EXTEST.

Carol – SAMPLE is intrusive to Mission Mode. And high speed IO. Having SAMPLE is a real cost to carry sample on these pins.

Carol – In EXTEST mode the standard receiver would be OO cell

CJ – figure 11-10 (of working draft) is a good example (modified figure) showing OO on each leg . The standard talks about redundant cells. If you removed OO here this would functional cells would still meet standard . Could relax the OO to need SAMPLE at these points.

Adam C – does this control or observe?

CJ –BC_4 ,input type. No timing delay just capacitive load that added.

Ken- OO cell listening to leg. Why is it hard to support SAMPLE and not hard to support EXTEST

Carol – path to OO has gating logic that is powered down during mission mode. In EXTEST mode you are being intrusive and not a problem causing signal integrity issues in EXTEST. In mission mode you don't want to disturb the signal integrity

Ken – if there is an OO cell that is being covered up listening to the leg , during SAMPLE that capability is turned off. And capture latch is not going to get any meaningful data during SAMPLE.

Ken – don't have a cell that reflects that SAMPLE is turned off. Need a BC_4 “prime” that would reflect this state. Need a new cell to show that SAMPLE is turned off.

CJ – another approach could be... Deprecating the need for SAMPLE on OO cell. Not sure the CELL is the answer. For function type OO relax need for SAMPLE. INTEST is a mirror image. INTEST is relaxed on cells with function clock. Cells of function INPUT require the mux, the control to support INTEST. So it is similar, cells of function OO would not need to support SAMPLE, where inputs would..

CJ – only change would be coding “BC_4, port, input” in BSDL instead of “BC_4, port, observe_only”

Carol – did this before. But had BC_4 OO. New devices would get BC_4 input BSDL change

Dave – in dot 6 JTAG is optional in mission mode.

CJ – required in 1149.1 though.

Carol- Mission mode receiver is still problematic

Linkages / Powerup / Powerdown

CJ – Current key words are : Analog_in Analog_out Analog_BIDIR

Analog_BUFFER POWER1 POWER0

Carol - how to code up a ref voltage.

CJ – power 1

CJ – Ok with not knowing what the voltages are .

CJ – DDR3 has VTT termination built into the chip so those voltages are not going to be used as much

Adam L – if point is to distinguish power and ground than lets use those terms. Power0 is associated with logic 0 and Power1 is associated with logic 1. VTT does not

apply to power1. Could be POWER_OTHER ? What do we do with negative voltages?
Can't be lumped together with power_0

CJ – negative power today is associated with Analog needs. Not logic.

Roland – Doesn't like power_0 term. Would rather call it GND. Makes more sense.

Carol – anything we make a key word we can't name pins that.(good point)

Adam – GROUND is usually never used as a pin name.

Adam L – Analog _ use of Analog term seems to deprecate 1149.4.

CJ – middle ground since Ken's input was Analog rather than Linkage. No preference at this point from me on the keywords.

Adam L- Happier with Linkage. Linkage is something that is already common.

Ken – sympathetic to Adam's point. Likes the evolution of Linkage keyword.

CJ - if we leave "linkage" than it may be the catch all again

Adam C – if you leave linkage and all the other key words will be market driven and everything will fall out.

CJ – no . market doesn't move fast enough. Could take many years for that approach to solve things while people still feel the pain. Test is only a small part of the market 'force' which would work on this. We can make the right choice just need to understand what the need is.

Ken – label on standard package in BSDL is the way you govern what level the language is at and if you accept new words. If someone wants to be lazy they could continue coding in the older BSDL. Can't claim compliance with latest BSDL requirements. That would be the risk they would take to be lazy.

Adam C – other risk they loose all the other benefits so new feature would not be available due to older BSD.

Roland – wouldn't that be motivation to update to a newer language.

Ken – new language would remove the world linkage and add new words to cover cases.

Francisco – true linkage cell still exists.

Ken – a keying pin possibly.

CJ – could be labeled as an analog in.

Ken – not connected to anything

CJ – 2 choices.. don't say anything about it. Or new * notation to call it out as a

NC

CJ – hasn't heard compelling reason to leave linkage in BSDL language.

Carol – LINKAGE_OTHER? So they would have to at least look at it .

CJ – doesn't seem to solve problem. Want to prevent people from coding with "linkage" like keyword and using it as a catchall. Need to force people to have to describe all pins and provide more information.

Ken – need to offer guidance for odd pins to help community to code correctly

CJ – we can write more examples.

Ken – has seen odd pins on Intel chips there for mechanically only. What are they called? Linkage other?

CJ – if we don't have enough key already words maybe you are against masking it's true functionality . not much you can do with Linkage_in, Linkage_bidir in the tools.

Ken – just need to offer guidance.

CJ- what I hear is LINKAGE_OTHER.

Francisco – seems to fall back to linkage problem. If we use LINKAGE_OTHER we will have the catch all again.

CJ –correct, I agree.

Roland – in a board level test environment. There are older chips that use older BSDL. How does that work for board tools.

Ken – tools have that problem today.. Look at the title of the suffix package. Tools change rules for each chip based on the BSDL.

Summary of key words thus far

CJ – I sense the WG is not happy with word ANALOG_ *function* as a key word. Reverted back to Linkage_ *funciton*. Still confused as to what the positioning pins (odd pins not electrically connected to anything) would be labeled. Still a little unsure about using Power1Power0 . may need to add POWER_OTHER. Also may want to use keyword GROUND.

Definitely Analog_ *funciton* is out.

General consensus is that “linkage” key word is not available. But not sure how to cover the odd pins like positioning pins.

Meeting adjourned at 12:04EST.

Next Meeting: March 16th 2010 11:00am EST

Current Issues listed and who will champion that issue.

- 1 Observe only. – Ken and Carl
1. Directionality linkage. - CJ
2. Power Pins. - Heiko
3. Pairing power pins with functional I/O - CJ
4. Sample / Capture. – Carol (Freescale) & Roland
5. TRST included in PCB level diagram. – Adam L.
6. Slow to Fall/Rise signaling issue – CJ
7. “No Connect” – Ken and Francisco.
8. Device ID – Still needs work
9. Low-Voltage self observe shorts coverage problem – JJ & Intel
10. Init – Carol & Carl

Action Items:

- CJ will post 1149.1 draft on website with line numbers to make it easier to refer to items in discussion
- Comment #10 CJ will take action to look at possibilities to add to the 1149.1WG website a document which shows which standards are based on 1149.1
- Comment #8 CJ will make changes to draft for observe only
- Comment #7 CJ will get in touch with Doug to get input regarding Comments

- Comment #5 CJ will Add a figure and little text to address TRST use with interconnection of components
- Comment #4 Adam L to add comment about TRST. Update figure 6.8
- Comment #3 Adam L will update language for any proposed change for this section.