

Date – 04/01/2011

Minutes of the IEEE-1149.1 Working Group Friday meeting

Attendees:

Dave Dubberke,
Adam Ley,
Brian Turmelle,
Carol Pyron,
Roland Latvala,
Heiko Ehrenberg
John Braden
CJ Clark
Carl Barnhart
Ken Parker
Wim Driessen

Meeting called to order at 8:30 am MST

Current Draft: [Still P1149.1 Draft 20110309 clean.pdf](#)

Agenda: (Informal)

Continuation of the INIT_SETUP rules discussions
Continuation of the PDL draft review

Minutes:

General:

Carl sent out an edited version on Tues. Only feedback from Ken so far
Carl hoping to get more feedback from Carol about the rules as structured so far.
Carl is working on Clause 8/9 updates and will send a new release next week.

INIT Discussions:

The first hour of the meeting was spent discussing INIT. Carl brought up the fact that initially we defined the init_data TDR to be a write only register shifted in from TDI. As we further developed the rules for INIT this past year, a special case was presented by Carol for voltage select pins that need the following flow:

1. The voltage select pins are of type 'Constant Value'. (New BDSL type)
2. They will have observe only BSR register cells
3. They will be captured and monitored by the init_data register also.
4. Checked in PDL code
5. If the captured values do not meet the expected states the test will be shut down to avoid damage to the circuit under test.

6. As long as you don't go to EXTEST, you have time to observe these pins and shut down the test without damaging anything.

There were subsequent discussions about how the expect value is defined in PDL. CJ mentioned concern about having an expected value for this register field but nothing to write into the register. So if there is an INIT_SETUP instruction and expect data defined the tools must manage this case properly. Additionally CJ said that if there is no default value assigned, the tool must then flag this as an error or warning.

Ken asked follow-up question to Carol about what happens in those special case pins are floating? What do you capture? If mid-band we don't know.

Carol confirmed that if the answer is wrong we want to abort.

Ken also clarified his point about some confusion on INIT:

1. There are now two ways to initialize:
 - a. Serially through TID to initi_data register (we all understand this flow)
 - b. Parallel capture of binary values into init_data register (read only for monitoring)

Carl took the action to revisit the rules for INIT and to add clarifications where needed.

PDL Discussions:

CJ showed a register diagram of data from BSDL from section C.8.2. for iWrite and iRead.

CJ walked through the states for Wim that PDL will typically follow inside the TAP state machine. CJ mentioned that RTI state is the typical starting point for iApply. Exception to this is after an iReset when TAP state machine moves to reset state.

CJ also discussed the affects of iEndState.

1. Noted that Pause can be used for overshifting the register
2. iEndState remains sticky until you change it.
3. The new iEndState will be invoked after the next iApply.

CJ took action to write this up further for clarification on the affects of iEndState.

Wim mentioned that the traversing of the state machine should be well defined.

Ken asked how 1687 is progressing on PDL. CJ said they are not working on it lately but they'll sync up later on.

CJ noted a couple things about 1687 usage:

1. iApply in 1687 does multiple operations behind the scene.

2. The tool providers load multiple instructions and do multiple scan loads to load all the correct values into the registers defined by iWrite.

Ken brought up the point that there needs to be caution used in the sequence of these operations for board level test.

CJ also noted that many people don't like this under cover activity in 1687. It hasn't been well discussed. Its ok when it works, but not so when a test fails.

Wim brought up point about correct scheduling of test sequences. Ken confirmed this order is important. EXTEST of 3 IC's is order dependent.

CJ pointed out that a register may get written 10 times during one of these iApply operations.

Wim asked about Ready and Busy bits. – iApply until done or error? Loop until ready.

CJ said lets start with the basics first. Perhaps add a parameter to iApply.

Meeting adjourned: 10:00am MST

Action Items:

- Carl to release a new full draft this coming week.
- WG members to review and provide feedback

Next Friday Meeting:

- Next week Friday April 8, 2011