Date – 01/07/2011

Attendees:
Carl Barnhart,
CJ Clark,
Dave Dubberke,
Ted Eaton,
Adam Ley,
Ken Parker,
Carol Pyron,
Roland Latvala
Francisco Russi,
Brian Turmelle

Excused: Heiko Ehrenberg

Agenda:

1) Continue review of IC-Reset Instruction.

Meeting Called to order at 11:30 am EST

Minutes:

Overview: Carl presented draft of IC_Reset rules and permissions
(document version: IC_Reset_20110106.doc)

IC-Reset Instruction:

- Rule c): thought to be too long and wordy. Carl to review.
- Rule d) discussion:
- Carol/Ted –
    - What logic functions are preserved?
    - Clamp persistence
        - IC_Reset
        - System Reset I/O pin
        - Only resets in this register, or other control bits too? (pll cntrl)
- CJ – If someone doesn't want Camp persistence, but only wants IC_Reset, can they still control PLLs from this register?
- Init_data register is now only persistent if Clamp persistence is in 'On' state
- Ken – Flow
    - POR
    - Init Setup/Run
    - Extest (garden varity)
    - Clamp Hold 'Off'
    - IC_Reset & Persistence 'On'
    - Clamp Hold 'On' holds I/O data and I/O analog control
- Carol – TRST_B and IC_Reset TDR

- Carl – IC Reset pins with BC_4 combinational, if BC_1 then 'test state' blocks the internal reset today.
    - Chip designers choice
        - BC_4 not blocked
        - BC_1 blocked by reset-select register and IC_Reset instruction
- CJ – Carl did you read my latest doc? Carl will read and follow-up.
- CJ – Different scenarios:
    - Some IC's don't have a TRST* pin
        - Don't implement IC_Reset
- Carl – Only an issue if we mandate it rather than a permission
- CJ – If everything is optional then designers skip the hard stuff
- Ted – This is not fine. Write the rules as blocking the primary Sys Reset I/O pin(s), but give permissions not to.
- Carl – Let's table this discussion for now.
- Roland – Perhaps give 2 bits in the IC_Reset register. 1=blocking, 2=non-blocking of primary Reset I/O pin(s)?
- Ted – If TRST* has an open then board will not work.
    - Put internal pull-down on TRST*
    - Motion to add a pull-down on TRST*
- CJ – Note there was no 2nd of this motion
- Carol – motion thought to be somewhat in jest.

Reset-Select Register:

- LSB – Master bit
- Polarity of reset select register should be addressed further to avoid confusion to the user
- Discussions of rules B and C of reset-select register:
- Much discussion of the common practice of asserting TRST* or TMS to reach TLR tap state.
    - CJ asserts the Std never intended for TRST* to be used other than at POR to initial the TAP controller the first time
    - Ted/Roland/Carol each attest to the common practice of assrting TRST* in industry today
- Carl gave his opinion that Clamp Persistence Controller should be renamed Test Persistence Controller. (controlling system I/O logic from test logic).
- CJ – PDL IResets removal by test engineers?
- Ted – IC_Reset persistence beyond TLR still may not work.
- CJ – Not following
    - IC_Reset – stand alone
- Ted – PDLs from different persons, pll settings from one, IC_Reset from another engineer.
- Adam Ley – This is a new 'State' of the machine. Perhaps overlay with Clamp Persistence
- Carol – We've run out of time. Continue to discuss this coming Tues.

Meeting adjourned: 1:00pm EST.

Action Items:

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Next Tiger Team Meeting:

- Next meeting Jan 14, 2011