

September 10, 2010

Minutes of IEEE 1149.1 - Initialize Sub-Group Meeting

Attendees:

John Braden
CJ Clark
Ted Eaton
Roland Latvala
Ken Parker
Carol Pyron
Francisco Russi
Brian Turmelle

Minutes:

Started with review of CJ's latest draft of the Std.

- Discussions of register fields associations and formatting and layout of that section in the body of the Std.
- Discussions about use in package file vs. inline in the BSDL
- CJ would like to see good examples for the Std so that future readers can clearly understand the concept of hierarchy, chain concatenation, using the segments from the package files, etc.
- CJ mentioned possible 'chain order attribute' to clarify this.
- Carol raised the question about whether or not we need to separate register_fields attribute into two versions _flat and _hierarchical as other way to clarify this.
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Francisco asked for clarification on the BC_6 removal:

- CJ is planning to remove BC_6 from the Std, unless there is a technical reason to keep it.
- Carol didn't see the need to remove it completely from Std, but plans to move toward BC_7.
- Ken agreed it is time to get rid of BC_6
- This moved the topic of the meeting into general discussion of self monitoring differential bidirectional IOs. CJ provided discussion of using PCIEX recv detect circuits as place to incorporate BC_7 BSR cells without need for additional test logic overhead.
- Carol discussed custom 'bidir' pads that use two signal ended drivers with a diff receiver. Carol agreed to generate a diagram of future discussion.
- Ken raised the point that detection of shorts at the TX output pins is the goal of the BC_7. Designers need to be aware of this, through a 'Rule' or strong recommendation, to run Spice sims to confirm their detect circuits really work for self monitoring.

The meeting ended on time.

Current Status:

Formalize Rules – In progress.

BSDL Constructs - – BNF coding in progress, semantic checks in progress.

Formalize PDL constructs – We need to start on this.

Actions:

- Carol to provide custom bidir IO example diagram.
- Roland to discuss SAMPLE issues related to Serdes pins. Tentatively next week.

Work still to be done:

Formalize side-file language.
Incorporate INIT into 1149.1 Std.

Next meeting date:
Same time next Friday September 17th.