Date – 08/12/2011

Minutes of the IEEE-1149.1 Working Group Friday meeting

Attendees:
Dharma Konda
Brian Turmelle,
Carol Pyron,
CJ Clark,
Dave Dubberke,
Ken Parker
Craig Stephan
Adam Ley
Wim Driessen
Josh Ferry
Heiko Ehrenberg
Francisco Russi
Roland Latvala

Meeting called to order at 8:35 am MST

Current Draft: P1149 1 Draft 20110722.pdf (_clean.pdf)

Agenda/Overview:
- Continued discussion of Linkage pins
- Continued discussion of VRef Port Associations
- Ken asked question on BC_10

Minutes:

Linkage Pins and VREF Port Associations

Carol opened the meeting today with discussion of linkage pins for ground connections:
- Power_0 should be ok
- Carol pointed out the rules about not using reserved keywords for signal names..
- CJ had thought that naming the keyword GND would be ok for parsers too, but since keywords cannot be reused for signals that idea was discarded.
- Conclusion of this discussion was that ground pins would remain POWER_0 types in the new Std.

Ken showed email of pros/cons of the various alternatives
- Put new keywords in port statements and remove 'linkage' altogether.
- CJ asked to stop this discussion and stated this should not be an issue.
  - We should not worry about older parsers

    - By leaving as is we are supporting in-house tool vendors
    - We have very complex pin map today so alpha/numeric pins would be more complicated
- Heiko – Let's keep in place where linkage was before and issue warnings if tools run into older 'linkage' keywords. This means tools still have to understand the old keyword linkage to flag with warnings.
- Ken – Looking at the pros/cons email I don't see a clear choice.
- Dharma – When we define analog_gnd analog_pwr as keywords how are we going to deal with new keywords that come up.
- Carol – In the new draft you will have the option to put a boundary register cell on one of the new linkage type pins. This will help with debug of the board. (linkage_in, linkage_out)
- CJ – Take a look at the new draft, added VREF_IN and VREF_OUT
    - One person is trying to add all this into the pin map. (Table B.2-Pin types)
    - This has not been fully thought out
- Carol/Ken – I think the multiple pin mapping problem leans towards not putting it in the pin map section.
- Ken – I think Dharma was asking: What about new linkage types that haven't been thought up yet? Which 'linkage' type is the catch all?
    - The temptation now would be to call everything linkage bidir.
- Carol – The linkage power types are not hard to work with
- CJ – The vendors are already stripping out information to give us 'linkage'
- Francisco – For automation we put it in the pin map file. For user information we put in the BSDL
- Carol – Why put it in the pin map file? That is for machines only.
- CJ – We recently added VREF_IN and VREF_OUT. It is hard to get into BSDL but it is defined in the data sheet.
    - We also need in machine readable format
    - Today there is no good way to associate VREF_IN and VREF_OUT with the pins they are used with
- Carol – We haven't discussed the capture value associated with the linkage pin types
- Carol – Capturing at a boundary cell on the POWER_POS pin internally.
- CJ – Yes you can put an observe cell on any pin. This is different in figure B.2, here we are trying to monitor power ir drop.
- Carol – We have to know is this IP powered up or not? It's on a power plane not a specific pin of the chip.
- CJ – Ken was saying we should leave the linkage pins in the port statement. Wim weighed in. Anyone else?
- Francisco – We have a design with a bsr cell but the package is not connected to the board.
- CJ – A real IO in the die which is not bonded out, but it has a bsr cell, but the package has a connection.
    - Port type :IN
- Dharma – For multi-chip modules we make it an internal cell

- Francisco – They are internal cells, but if the package has a pin
- CJ – The pin map string already has addressed this with the 'asterisk' which says the pin in not bonded out. We now have the ability to have multiple pin maps
- Carol – Yes, we have big package, little package and bond differently for different markets.
- CJ – Sure, low cost packages with limited bond out
- This is a tangent to the pin types.
- Back to table B.2-Pin types
- Heiko – I'd prefer to keep in the port map
- Carol – Yes agreed
- CJ – Ken send me updates for the wording to help clean up.
- Carol – You had mentioned GND : GND would be ok. You cannot use the keywords for anything else
- CJ – Yes, I was incorrect. The keyword cannot be used as a signal name. We are stuck with power_0
- Carol – Any other comments on linkage? Ken will give us feedback.
- Francisco – What about inout vs. LINKAGE_BIDIR (change to linkage_inout).
- Carol – Josh?
- Josh – Nothing to add at this time.
- Adam – I think additional work is needed for LINKAGE_xxx and POWER_xxx pins. The types themselves need some work still
    - VREF_OUT there are different kinds. Maybe/maybe not an issue
    - VREF_OUT based on zener or resistor divider, or power mosfet
    - Similar for POWER_POS and POWER_NEG, there are power into the chip and power out of the chip based on the chip type.

- CJ – True these are power input pins.
    - Power output pins would be VREF_OUT or LINKAGE_OUT with a disable method if you can turn the power off
    - Even the old one could use some definition cleanup. (in, out, buffer, inout)
    - How can knowing this improve the test experience

- Adam – True we thought we had it nailed in 1990 with LINKAGE
- CJ – Agreed, but the added capability gets us further than we were
- Carol – Two final comments:
    - Do we want to in the description of LINKAGE_INOUT use this to cover future bases if no other category fits well?
    - For a ball on a package that is no connected to silicon at all, or not to the board at all? What classification is this in the pin map. It is not for heat syncs.
    - CJ – This should be LINKAGE_MECHANICAL. Non-electrical use. Any and all non-electrical use
- CJ – What about optical IO, we are entering diminishing return

- Ken – If I have a current source pin, do I call it LINKAGE_IN since VREF_IN doesn't really match? Are we happy with VREF or call it REF t make it more generic?
- CJ – I'd call it VREF_IN. Should we call it REF_IN and REF_OUT?
- Adam – We once had a power port association. Is that still there?
- CJ – No, we have a register port associate, but not a power port association. Are you saying make the VPA (vref port association) less restriction?
- Adam – Yes.
- Carol – Yes, we haven't discussed this.
- CJ – Power or Vref port associations.
- CJ / CJ – Adam I can go look into the broader scope.
- Adam – I was just thinking power port association could be just as important as vref port association
- Ken – If there are lots of power pins on a plane then then the power port association is less meaningful.
- Carol – We have avdd and small planes, and also large planes, and common grounds.
- CJ – My thinking was VREF as associated with an IO
- Carol – Internally the DDR diff IO has a diff receiver and the VREF goes to all of them as the common mode point. There is also a power GVDD to the DDR IO cells
- CJ – Yes this is very typical.
- Carol – You thought this wasn't very interesting. Can I associate by bit vectors or call out individually?
- CJ – In the prior case where we are listing pins associated with a register that may have faults associated at the board level. For DDR the VREF is pretty obvious. Ken – You could use both powers and vrefs?
- CJ – Yes.
- CJ – Folks ok with this? (The WG generally agrees with PPA)
- CJ – OK I'll do a little more work on it.

Ken's BC_10 Question

- BC_10 defined as output3 function, but is bidir in port statement
- For self monitoring cell is it ok not to have an input cell on the pin?
- Effectively a self monitoring output promotes itself to an input for EXTEST purposes
- Carol – What does it capture when it is acting as an output?
    - It doesn't say what does it capture when acting as an input
- CJ – True there is no short cut when tools don't read the meaning of the cell. This is an oversight calling this an inout. All tools don't read the content of the boundary cell
- Adam – Pins of port type buffer also can be self monitoring
- B.8.14 rule is written for that purpose. For an output3 this is a corner case and has no connection to the system logic. We shouldn't make changes

- Ken – I'll need to fix the 1149.8.1 standard anyway.
- Carol – If the only sync is the boundary cell there is no connection to the system logic, so this isn't really a bidir.
- CJ – Good we closed these two issues.
    - I"ll work on PPA some more.
- Carol – I did not get a chance to write up how the relax SAMPLE yet.
- CJ – Hurry up before you lose momentum. ☺
- Carol – There has been good discussion on this this week.

Meeting adjourned: 10:00am MST

Action Items:

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Next Friday Meeting:

- Next week Friday Aug 19, 2011