Date – 14/Oct/2011

Minutes of the IEEE-1149.1 Working Group Friday meeting

Attendees:
Adan Cron
Bill Bruce
Brian Turmelle
Carl Barnhart
Carol Pyron
CJ Clark
Craig Stephan
Dave Dubberke
Dharma Konda
Francisco Russi
Heiko Ehrenberg
Jeff Halnon
John Braden
John Seibold
Josh Ferry
Ken Parker
Peter Elias
Roland Latvala
Sankaran Menon
Adam Ley

Meeting called to order at 8:30 am MST (AZ)

Current Draft: P1149 1 Draft 20111001.pdf

Agenda/Overview:
CJ presented slides on Power/Mux (version 5) for Segmented TDRs and Boundary Register

Minutes:

CJ explained that having the BSR and INIT_DATA in the always-on power domain could cause a large separation of the logic from the I/Os as well as a large number of wires and power isolation cells on the edge of a powered-off domain. This is expensive in terms of design effort, area and pins of the edge of the hard macro. (Slides 11 and 12)

Ken - Asked for clarification of CJ's diagram

John Seibold – I'm not convinced a test engineer couldn't debug this without segments. It's fairly common problem to see a bank out due to power missing from a segment due to a regulator.

CJ – You may have ways to determine this but we don't have fixed breadcrumb bits at board test. Segmented boundary register could also support segmented EXTEST on part of the board. Two TDR cells needed:
Power cell
Mux

Carl – We probably want to reference the Power Std if we are going to talk about it here.

CJ – Agreed

CJ – Showed BSDL example. Like commenting out a register assembly segment, the tool can know the length changed when a segment is powered down.

Register_Mnemonics
DOMAIN Cell – Responsible for sensing and overriding power
MUX
POWER
CONTROL (normal and override).

Register_Assembly
Mux is a 0bit element to tell where a segment begins and ends

CJ – Reviewed basic rules/operation

Carl – You showed on prior slide default rules for a domains behavior, here you say each segment is always collapsed.

CJ – After TLR the mux is always off.

Carl – The length then is the collapsed length? Default in the BSDL.

CJ – Correct.

CJ – New attribute BOUNDARY_REGISTER_SEGMENT

- Name each segment (east, west, north, south for example)
- Cell counting is local to a segment. Should be easier than counting all the cells.

Carol – If a domain is powered off by a board instance. Should we have another power mux to tell you that you can never power that domain up?

CJ – For an IC vendor there is no issue. If you want two keywords external and power that might be possible to make it easier to understand.

To avoid BSR from getting corrupted due to mux control bits, we already allow internal cells. If internal cells specify values of 1,1 and you load 0,0 all bets are off today.

Carl – CJ you have to specify SAMPLE or EXTEST for the boundary register.
CJ – Correct.

CJ – Also Sankaran and I discussed iRunLoop command to wait for power to come on. I'm not sure that is needed.

Heiko – If those 4 power muxes are on different power domains how does it power up.

Carol – Each power mux is in an 'always on' domain

CJ – If only 1 pin comes into the IC it is still a concern

Sankaran – I think segmented capability is really required and multiple bits. The iRunLoop is required.

Carol – You are asking for multiple bits to turn on a domain?

Sankaran – Yes.

CJ – Let's think about that. It may be more complex than it needs to be. If we need PRELOAD and SAMPLE to execute these it could be too complex.

CJ- How much time are you talking about to go from OFF state to ON state? So we have a time frame of how long you expect to wait.

Sankaran – In 'us' range.

CJ – Let's think about this, folks will want to quickly get into EXTEST.

Ken – If I have 50 power domains in my device, what are the requirements for sequencing them with scans to power up correctly.

Sankaran – It's probably done in parallel. Today we look at the chain flat. Segmented chains are a good idea going forward.

CJ – If we restrict to not allow sequencing is that ok?

Sankaran – Yes.

Ken – I would want to turn them on one by one to find a fault.

CJ – During bring up you may need to back off.

Carl – The Std assumes IO domains can be brought up in parallel. There are various mechanisms to allow for sequencing power. However IO domains can be brought up in parallel or in sequence.

CJ – Ken and Sankaran are asking two different questions.

CJ –
PDL tool should do:
Turn on power to a domain
Check domain is on
Turn on the mux

Carol – Poll until a bit is set.

CJ – Yes, could loop until conditions Sankaran mentioned are met.

Ken – Is this a sing

Sankaran – What is the solution? Multiple iRuns?

Carl – Annex C there is a polling mechanism to wait for all iRead expects to become valid. It compare the two fields until the compares pass.

CJ – Others?

Carol – We originally brought this up for Init-data, now for boundary register.
You would have to power up for Init-data first, and may not need to do again for boundary reg.

CJ – Correct. If you require sequencing to run Init-data before

John S. – The power status cell. Are we assuming the status will always be available?

CJ – I don't see how we could get by otherwise. We need a control/sense power cell, also a sense only power cell

Josh – Is this restricted to boundary register, or allowed for all TDRs.

CJ – All TDRs

Carol – Except IDCODE and ECID.

CJ – As yet to be defined.

Ken – If I have power domain control in the init-data register, the two bits that control this. Which domain are they in?

Carol – If Serdes has init-data and boundary register. Both require a power/ mux in front of it. When you get to boundary register you may have already turned on the power during init-data.

Ken – So there is an OR gate to turn on the power to a domain. (init-data and boundary)

Sankaran – Maybe monitor all bits and turn on as needed.

CJ – There could be two methods or gated. You'd still need the power mux in there. Otherwise if you do flat, you have to hope the power is on.

Ken – Sure

CJ – If you have power muxes in both, then you are turning a switch to turn power on that is already on. No harm done.

Carol – When you have an off die digital voltage regulator, there is no way to tell that certain pins will toggle the on-chip power.

CJ – Board level constraints should manage this?

Carol – Real world case, customers toggle the pin, and we get calls saying boundary scan breaks.

CJ – Showed 3D is memory stacking example. Requested Tues meeting starts ½ hour earlier. What is the next step?

Adam L – My sense here is that we would benefit from subject matter experts here. I credit CJ for his examples, but I don't think we have a deep enough understanding of the issues. Boundary register segmentation may be a good idea, but I'd like to have a deeper understanding for experts in low power design.

CJ – That would be great to get some experts.

Carol – That is good idea. We are out of time for today.

Meeting adjourned: 10:00am MST (AZ)

Action Items:

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Next Friday Meeting:

- Next week Friday Oct 21, 2011