Date – 16/Dec/2011

Minutes of the IEEE-1149.1 Working Group Friday meeting

Attendees:
Adam Ley
Brian Turmelle
Francisco Russi
Carl Barnhart
Craig Stephan
CJ Clark
Ken Parker
Roland Latvala
Peter Elias
Dharma Konda
Carol Pyron
Dave Dubberke
Jeff Halnon
Ted Eaton
Heiko Ehrenberg

Excused:
Bill Bruce
Josh Ferry

Meeting called to order at 9:35 am MST

Current Draft:

Agenda for today:
1. Carl addressed INIT changes
2. CJ provided an update on PDL

Minutes:

INIT Review

Carl stated new draft available on website now. Init_Run Execution attribute was dropped.

Carl discussed that we also have the IC_RESET instruction that can do some of what INIT was intended to do, but that we need to revisit the new features since we added INIT and determine if the INIT rules are still sufficient or need tweaking.

Carol added that PDL can apply a wait state and this may be all that is needed in some cases so INIT_RUN wouldn't be needed in such a case.

Roland asked about INIT_SETUP changes. Carl/Carol responded that due to the inclusion of segment selection bits into the init-data TDR, that the former use model of a single init-data scan during INIT_SETUP is no longer possible. Multiple scans will be required to determine power status and to correctly bring up a chip. This all impacts the former use model of init-data with a single scan. The rules for INIT will need updating.

PDL Review

CJ said he wants to make sure we get a good dialog going. Peter had some concerns. We want to make sure all the issues are understood.

CJ said this material is on the web so will share the pertinent material today. This is. material he presented at ITC.

Ted asked about the ITC material. Was it his view point or the WG's. CJ confirmed it was his own view point.

CJ reviewed his slides and discussed the ecosystem around the IC

IC Tester (perfect env)
IC in System (commodity components)

One purpose of CLAMP_HOLD and IC_RESET is to facilitate reuse of the IC tests at the Board test level, to avoid sending IC's back to vendor. This could save time, trouble and cost of rework. We can identify if we have a problem in system. Benefits industry all around.

We'd like the ability to describe things (language) across the industry.

IC ecosystem, neighboring ICs, DDR, Serdes. Domain expertise is needed. Reuse of IC level bist tests can be very advantageous and provide benefits to board test space.

CJ sees board test as more than EXTEST. High speed connections can fail Serdes bist and pass slower EXTEST.

3D stacking of die also poses test challenges.

If 1149.1 can provide guaranteed test success there is benefit in this.

3D reset issues, and also at system level too.

1149.1 requires a TDR to talk to IP blocks, 1687 may or may not.

Ted responded that all slides up to this last one were in the PAR of 1687. Ted has concern about picking out parts of 1687 and putting them into 1149.1.

CJ and Ted differ on this in their opinions.

Ted feels it unethical for CJ as Chair to influence 1149.1 WG to adopt the 1687 pieces.

CJ does not see if that way.

Carol asked Ted about scan chain muxing, and power domain segments.

Ted said that once you have a feature it opens it up to multiple uses.

CJ commented that customers now have more choices in Standards, and vendor tool sets to choose from to meet their test needs.

Ted and CJ continue to debate reusing 1687 constructs and 1149.1 constructs across the two standards.

Carol tried to bring the group back on track discussing PDL.

Ted and CJ continued to discuss the 1687/1149.1 issues.

CJ's opinion is that IP domain expertise can be fed all the way through to the board test guys, or system integrators. He encouraged the WG to review the slides on the web. CJ seems to think 1687 and 1149.1 can coexist.

Ted asked to open for questions.

Carol asked if Peter had any comment to clarify his questions.

Carl commented that being an 1149.1 member only. He sees that 1149.1 owns up to the TDRs, not beyond the TDRs. We do not have any rules about what is beyond the TDRs. We manage the TDRs, and do not go beyond that. IC_RESET is the only exception. Some of the discussion is about things that are not in the Std itself.

Carol asked about descriptive text beyond the TDRs. Carl confirmed some simple examples are available, but may not be realistic, and this is not part of the normative standard.

CJ disagrees.

Carl added that we have not voted on PDL level 1 yet.

Dharma added that he is concerned about us focusing too much on the IC testing, and the possible impact this could have on the board test environment interconnect tests.

CJ responded that interconnect test is a small portion of board test today, only addressing stuck at faults. CJ wants to see the Std evolve with the industry and address the challenges of today's testing and user defined registers.

Carol confirmed that historically PRIVATE instructions handled the chip level bists, and so on.

CJ confirmed tool vendors also had private methods.

Back to PDL discussion:

CJ showed a SPI example proc as a simple example. Just an example of PDL level0 and level1 to consider benefits of PDL level1.

PDL level0 can only do simple expects, and multiple errors show up at the same pin.

For PDL level1 you have ability to have variables, and higher level commands. PDL level1 can then provide better diagnostics as a result.

Carol/Carl confirmed that higher level languages provide better test routines.

Peter had concerns about sequential operations. CJ showed that branching and parallel operations are also possible. For example 4 chips in a chain running together.

Carol added that Ken had documented these parallel chip operations.

CJ added that the iApply is the point where synchronization occurs.

Peter asked where is the TCL? CJ said this example is TCL and discussed the issues he sees. Merge-able procs vs. non-merge-able procs. Debug procs could be PDL level1.

Peter asked about PDL0/1 usage for board interconnect test vs. debug.

Carl added that board test vectors are not PDL. PDL is only for the setup portions.

CJ didn't fully agree with Carl. For PRBS it is a board test.

Carl clarified he was talking about board interconnect tests, not PRBS tests.

Any final comments?

Ken said he will send out the table Carol mentioned. For simple model it was correct, but for multiple scans it will be considerably more complicated.

Carl asked Ken to revise his table for these more complex cases we have now with multiple scans.

Carol asked the WG to read the draft over the holidays.

Carl said PDL is not fully defined in the current draft and that will need to happen after the holidays.

Heiko added that PDL level1 is much better than level 0 for CJ's SPI example.

Meeting adjourned: 11:05am MST

Action Items:

- WG to review the latest draft over the break.

Next Friday Meeting:

- Friday meetings canceled for Dec23, 30.
- Next Friday meeting is on 06-Jan-12

Happy Holidays!