

Date – 12/17/2010

Attendees:

Carl Barnhart,
CJ Clark,
Dave Dubberke,
Ted Eaton,
Heiko Ehrenberg,
Adam Ley,
Ken Parker,
Carol Pyron,
Mike Richetti,
Francisco Russi,
Brian Turmelle

Agenda:

- 1) Review of IC-Reset Instruction

Meeting Called to order at 11:30 am EST

Minutes:

IC-Reset:

- .Carol showed a copy of the IC_RESET straw-man document.
- Rule b): change verb to “assert”
- Rule c): Rewrite to clarify the assertion of the reset signal.
- Dave: Use of TCK only doesn’t work for some – Intel needs system clocks for resets. Mike agreed.
- Carl: Only specifying the width of the reset signal pulse, not specifying the time needed for the reset itself.
- CJ: If Clamp-Persistence is on then Resets may (should) be blocked, but not system clocks which must be on for functional reset.
- Ken: Test engineer needs to know that system clocks must be on; they are routinely shut off for board tests now.
- Carol: Do we need multiple max TCK freq specs? By instruction, or TDR, or TAP state?
- Ken: Standard does not specify which element in the test logic limits the frequency of TCK, so even user instructions must abide by spec limit even if desired to go faster for a user test.
- Ted: We go faster anyway for internal tests.
- Ken: How would you handle heritage devices with only single spec and mix them with new chips on a board?
- Carl: Time specs and frequency specs are an open issue in general and specifically for INIT_RUN and IC_RESET. Let’s table for now.
- Carol: does the Standard require that TRST* processing be completed within one TCK cycle?

- Carl: No. A TCK cycle can be infinite, so would not mean much anyway.
- CJ: Let's be careful about feature creep. we are not trying to fix all the warts.
- Carol: Rule e) is difficult because some of the INIT_RUN results may be in functional flops.
- Carl: True, but designer needs to pay attention. Some resets (for MBIST, for example) will not need to disturb the I/O. A master reset might be incompatible with Clamp-Persistence.
- CJ: In CPC schematic, we show Clamp-Persistence intercepting a SysReset signal to illustrate that some resets or some portions of a reset may need to be blocked by Clamp-Persistence.
- Mike: Complex chip resets require multiple resets to be asserted in tightly controlled sequences, and sequence may have to be altered after first silicon.
- Ted: If we drop the RTI requirement, and turn reset signals on and off with reloads of the TDR (Shift-DR), we have full control of the reset sequence even after first silicon. Clear TDR with Test-Logic-Reset TAP state, otherwise persistent. Sometimes want to hold functional logic reset during testing.
- CJ: We have a number of new TDRs that have persistence requirements and we need to make sure that this is documented.
- Ken: We still have a multiple IC problem with coordinating individual chip resets. Can we count on a master chip that controls the entire board reset?
- CJ: Still should have LSB as "Master" reset (defined by user). Reset can be asserted on multiple chips at the same time, but we cannot control when they come out. The can also be run sequentially.
- Carol: This was not intended to be only a full reboot. What resets may be triggered and what they do is up to the chip designer.
- Ted. We need PDL to control all this either way.
- Carl: PDL at the chip or at the board level (INIT PDL is for an instance of a chip on a specific board.)
- Carol & Ted: There would be chip level PDL for resets.
- General consensus that Ted's suggestion is preferred.

Meeting adjourned: 1:00pm EST.

Action Items:

- Action item taken by Carl to modify the straw-man set of rules for IC-Reset per Ted's suggestion.

Next Tiger Team Meeting:

- No more meetings this year. Happy Holidays, all!
- Next meeting Jan 7, 2011