Date – 01/18/2011

Attendees:
Carl Barnhart,
Adam Cron
CJ Clark,
Dave Dubberke,
Heiko Ehrenberg,
Adam Ley,
Ken Parker,
Carol Pyron,
Roland Latvala,
Ted Eaton
Francisco Russi,
Craig Stephan,
Wim Driessen

Excused: Mike Ricchetti

Agenda:

1) Required Patent Disclosure Slides
2) Reminder on discussion etiquettes.
3) Finalize IC_RESET

Meeting Called to order at 9:00 am MST

Minutes:

Overview: Carol presented overview of Friday's call. CJ then proceeded with explanation of the drawing of IC_Reset reset-select register and discussions followed:

- Ted – What is the TAP POR?
- CJ – TAP POR on chip when TRST* pin is not present. (can have both)
- CJ - Many ways to implement TAP POR (pll lock, power supply ramp, macro)
- CJ - Update stages can be set during TLR state if FF1 reset hold flop is set.
- Adam C. - Is this a case where we have grades of compliance?
- CJ – No I don't think so.
- Ted – Why are we not using the Test Persistence controller?
- CJ – The reason they are divorced is that we don't want to clamp the pins at the same time we control the resets.
- Ted – Why not make it a global change to the state-machine so that everyone can take advantage of this new methodology? Why is this not global?
- Carl – Test Persistence controller does not preclude using with a user tdr. Once ON the chip stays in its safe and cool state.

- Carl – They may be some cases where you want to control the resets without clamping the IO
- CJ – Review of CPC controller diagram. Pins are clamped so limits what you can do with IC_Reset. Allows us to not have to pair with other test mode instructions
- Carol – We could have a separate instruction that is an expansion of CPC that can set persistence then could be overridden to control Clamp Hold and IC Reset. This is a persistence that may need to be orthogonal and expanded more in the future.
- CJ – The only way to have a Test Persistence controller is to separate it. Use cases may want simple method from Clamp Persistence controller or IC Reset.
- Ted – There is much more to resetting the chip than just the external reset pins. Why don't we have control over all the other registers necessary?
- CJ - We are trying to control the equivalent of the pins.
- Carol – IC vendors may still have User instructions
- Ted – Why not block TLR state globally to all TDRs at the same time.
- CJ – Not trying to address all TDRs in the chip at the same time. All we are emulating at the boundary is the interface to the outside pins.
- Ted – We have PDL and bus composition stuff already so a global solution is within reach.
- CJ – Trying to implement something within the time the group has.
- Ted – Just make a global state machine change. What do others think?
- Carol – Ted can you write this up?
- Ted – When you load this mode from the Jtag TAP controller this global mode could be implemented.
- CJ – Ted can you write this up?
- Ted – Possibly.
- CJ – CPC works pretty well
- Adam – Ted, when a pin is a system function the system reset is also a system function, you see PLLs and other logic are also global functions that need to be controlled. Is this correct?
- Ted – Yes, chips are brought up in functional mode.
- Roland – Can the use of the optional bits C,D,E,F… be used for PLL control etc. To meet these requirements?
- Ted – Those bits shouldn't be part of the reset-select register
- CJ – Is this too simplistic for some devices? Yes. Others it will suffice. You could put the extra bits into init data tdr, or also the reset-select register.
- Lost Carl's phone. But message through Ken was that Carl also would like to see Ted write this up.
- CJ – Do we want the reset hold bit?
- Roland – Yes for flexibility
- Carol – Yes it seems to work
- Ted – Yes a good idea. Draw a box around it and make it part of the TAP controller.
- Ken – Why is this bit excluded from the dashed boxes?
- CJ – A functional bit not cleared by TLR
- Carol – Give this bit an exception to rule 9.3.1c and proceed.

- CJ – It doesn't need an exception. We don't violate the rule unless I'm being creative with my interpretation. Anyone disagree? No objections.
- Adam L. – Suppression of TLR for Clamp Hold. Also suppression of TLR for IC Reset. A global instruction to handle this.
- CJ – We need to work this out. If Adam and Ted want to draw this up.
- Francisco – Do we have 2 new proposals? Carol and Ted?
- Carol – Not from me. I'm willing to drop it. We are getting close.
- Carol – Is Carl making progress still?
- CJ – No, this is a gating issue. Changing the CPC is a big issue. A global blocking bit requires more thought.
- Wim – Clamp deals with outside world of the chip, resets deal with insides of the chip. Combining them causes some question.
- CJ – If CPC is combined with IC Reset then more work to do and pins are clamped so you don't get the same effect. So combining the two is not likely. Separating a blocking bit of TLR state from another means is a possibility that would need further discussion, so we will not close this topic today.

Meeting adjourned: 10:00am MST.

Action Items:

- Ted and perhaps Adam L. requested to write up a proposal of a more global TLR blocking scheme.

Next Working Group Meeting:

- Next meeting Jan 25, 2011