Date – 07/29/2011

Minutes of the IEEE-1149.1 Working Group Friday meeting

Attendees:
Ted Eaton
Brian Turmelle,
Carol Pyron,
Roland Latvala,
Carl Barnhart,
CJ Clark,
Dave Dubberke,
Ken Parker
Craig Stephan
Adam Ley
John Seibold

Excused:
Wim Driessen

Meeting called to order at 8:30 am MST

Current Draft: P1149 1 Draft 20110722.pdf (_clean.pdf)

Agenda/Overview:
- Discussion of 'selected' definition
- Presentation by John Seibold of additional Init_Data register examples using package files, with register mnemonics, fields and assembly.

Minutes:

Discussion of meaning of 'selected' per the rules of the Std:

The WG discussed the meaning of the word 'selected' as used in the rules of the Std today, and asked whether or not this is sufficient. The Std currently suggests that only one register is selected between TDI and TDO.

The consensus of the WG is that in light of CLAMP and now also CLAMP_HOLD the descriptive text for 'selected' should also now differentiate what register is selected to be between TDI and TDO, and what additional register(s) may be being 'utilized' at the same time.

- Carl - Clause 8.1.1a – Any register 'not selected' shall not….
- But for CLAMP it selects two registers bypass and boundary. We need to make it clear 'a set of registers are selected' and a single register selected for shifting.

- CJ – You used to select a register and finish what you were doing. Today that doesn't occur. Start something in a register, go off and do something else.
- Carol – So with Clamp Hold and persistence stuff, it selects the bypass register, and then utilizes the boundary register from the controller
- CJ – We should add the word 'utilize' as part of the definition.
- Carl – I can do that, but be aware we are changing rules from 1993. The documentation clause isn't followed, but industry usage would allow us to change the definition.
- Adam – Selected means something more than just what is between TDI and TDO. There are a lot of things that are not documented in BSDL. As far as standard instructions go, it is mandatory. It is used as in 'selected for operation between TDI and TDO.
- I don't object to clarifying this if we do it carefully.
- CJ – BSDL doesn't allow you to describe this. There are many things not described in BSDL.You cannot describe selection of bypass in Clamp
- Carl – If we want to bring the wording into alignment that is ok. It was never explicit that Clamp selected both bypass and boundary.
- CJ – Yes these are old rules.
- Carl – Define 'the active instruction' to mean what is loaded into the instruction register. Is this ok?
- Carol – Yes, active until update-ir or next tlr state.

<u>Presentation by John Seibold of a new Init_data register fields example</u>

John presented new examples of a couple Serdes ip blocks that use INIT_SETUP instruction and init-data register:

Highlights of his presentation and the WG discussion:

- John used package files for field segments for each Serdes macro.
- Defined a package file
    - Mnemonics from data sheet
    - Rx term
    - Tx cm
    - Tx swing
    - MFG (Test) with **all bits** defined

- Ken – John is MFG test available at board test?
- Ted – I would suggest you need control over all these for board test.
- Carol – Yes agreed needed for chip and board test.
- John/CJ – It is based on your board whether it has ac-coupling or not and so on.
- CJ – This is an example of setting all the bits in the mnemonics as John shows.
- Ted – John you may want a reset default value.
- Carol – There may be no default. If someone loads all zeros the tool should kick it back at you and say 'fill this in'
- CJ – No reset values, when the chip powers up, there is something there.

- John – Correct, but not sure what. It needs to be initialized.
    - Two packages: serdesH, serdesO
    - BSDL – REGISTER_ASSEMBLY
    - A mix of SerdesO, SerdesO, SerdesH,SerdesO
    - MFG(Test) and BSTERM.DEFAULT

- Carl – I'll need more help to define the rules for 'all bits'.
- John – Updated register fields and added an ALLBITS field.
- Question for John from Ken – missing serdesH_init_data package. (typo)
- Ted – You can't use the package name as hier reference?
- Carl – package identifier is allowed.
- CJ – Yes that is correct.
- Ted – Not only does the complier need to find the package file, the user does too.
- CJ – He needs to know something about the package files.
- Ted – User did not write the BSDL.
- CJ – USING on each line is verbose but is ok.
- Ted – Imagine 10,000 lines. Use USING as John did, or allow a dotted path
- Carol – You could add serdes channel names.
- CJ – Yes, he's using i1 i2 i3
- CJ – I don't think calling out the instance 4 times is hard.
- Ted – Couldn't you use a colon (:) identifier?
- Carl – VHDL allows : so we wouldn't know when we have field or a package segment
- CJ – We should show an example. A package could call another package.
- Ted – General case true, but we should allow for pulling in any package file in the hierarchy.
- CJ – There will be limitations on the dotted package file.
- CJ – When we bring in the top level package file we call it out and are done
- Carl – I'm not so sure.
- BSDL
    - Package1
        - Package1.1
- I think it is ok as is.
- Ted I think you can do what you want.
- CJ – Let's put an example together for this dotted case.
- Ted – Thinking ahead 3 years for 3-D designs.
- Carl – The discussion of hierarchical packages should be tabled for now.
- Carol – Adam any comment?
- Dave – No
- Brian – No
- Roland – Agree with John. USING on each line.
- Ken – One concern – the lines could get long
- CJ – That's why we put it on the first line
- Ken – When we start nesting package files, how do we debug this?

- Carol – Pin pair, bank of serdes IP.
- Ted – 10-20 levels
- Carol – 3D aspects
- CJ – DFT engineer vs ICT engineer
- Ken – We have wording in Std to manage package files. This is left to the vendor and customer
- Carl – EDA users override default naming conventions anyway. We should leave it open.
- Ken – Should we offer advice.
- Carol – Recommendations
- Carl – Recommendations to use specific strings
- CJ – C++, Verilog, hundreds of files. If you overwrite a file you are out of luck. It happens today. We shouldn't need to spend too much time on this.
- We shouldn't specify too much here other than general guidance.
- John – The first time I wrote init_data.BSTERM
- CJ – No tdr.something is not allowed in PDL.
- Carol – Anything else?
- Carl – Ted's question, whether we should use USING on each line or only once and it gets inherited, or allow package file built into the syntax?
    - No formal vote today, we need an example of the package.hierarchy also.

Meeting adjourned: 10:00am MST

Action Items:
- Carl has posted new daft on the website for WG review

Next Friday Meeting:
- Next week Friday Aug 5, 2011