July 30, 2010

Minutes of IEEE 1149.1 - Initialize Sub-Group Meeting

Attendees:

Adam Ley
CJ Clark
Dave Dubberke
Roland Latvala
Ken Parker
Carol Pyron
Bill Tuthill
Ted Eaton
Carl Barnhart
John Braden
Bill Eklow
Francisco Russi

Minutes:

During this meeting we reviewed Carl's VHDL coding style example which included a package file for defining a sub-block and incorporating its hierarchical reference into the BSDL example:

- Questions about PDL. Ted to include Francisco and Bill in 1687 reflector.
- Carl's VHDL example incorporated a package file for defining the REGISTER_MNEMONICS and a new attribute REGISTER_SEGMENTS which define a sub-block of the full TDR to be instantiated multiple times in the REGISTER_FIELDS section of the BSDL.
- Discussion that the package file could be included using a 'Use' statement, or appended into the BSDL file, or by removing the header/trailer could be coded inline into the BSDL.
- Ken asked if there is value added in this?
- Ken/CJ mentioned BSDL has always kept package files separate, and that the BSDL annex would need reworking if that changes needlessly, so Ken would like this to be a consideration.
- CJ mentioned pro for using a separate package file, is that it can then be maintained and reused across multiple ICs.
- Carl walked us through his example, and introduced the array <> notation of VHDL that would have to be passed into PDL somehow. Carl asked for PDL experts (CJ, Ted) to help bridge from BSDL to PDL to prove out this example.
- Ted asked about bit ordering in the REGISTER_SEGMENTS attribute. Since bits may not be contiguous.
- Carl will look into bit vectors and also look into Ted's questions.
- VHDL 'Use' statement is like `include statement in verilog.
- Ted mentioned that PDL does not support instance array structures.
- Bill mentioned they do not have unqualified hierarchical levels in PDL.
- Fundamental problem is REGISTER_SEGMENTS use arrays, and arrays are not supported in PDL.

- CJ discussed there are some PDL statements which 1149.1 won't support, but perhaps the use of array's could be added.
- Possibly a mix of both CJ's and Carl's hierarchical referencing approaches.
- Carol mentioned that port associations were not addressed in the package file example
- Carl, stated the main idea is the need for new REGISTER_SEGMENTS attribute.

Current Status:

Formalize Rules – no activity this week

BSDL Constructs - – In progress.

Formalize PDL constructs – CJ, Ted, and Carl took action item to look into PDL coding for this example which used arrays.

Actions:
Carl sent out an update his VHDL example BSDL/Package
CJ, Ted, Carl to develop the PDL coding for the example

Work still to be done:

Incorporate INIT into 1149.1 Std

Next meeting date:
Same time next Friday Aug 6th