Date – 30/Sep/2011

Minutes of the IEEE-1149.1 Working Group Friday meeting

Attendees:
Bill Bruce
Brian Turmelle
Carol Pyron
CJ Clark
Craig Stephan
Dave Dubberke
Dharma Konda
Francisco Russi
Ken Parker
Roland Latvala
Wim Driessen
John Braden

Excused:
Adam Ley
Ted Eaton
Carl Barnhart

Meeting called to order at 8:35 am MST

Current Draft: P1149 1 Draft 20110820.pdf (_clean.pdf)

Agenda/Overview:
ITC Overview
Std status update
TDR cells (CJ)

Minutes:

ITC Overview:

Overviews from Ken, Dave, CJ, Carol, Francisco
Presentations CJ and Ken
Poster sessions Dave, Ken (dot 8.1) and CJ

Status update:

CJ – Segmented Init-data register and boundary register
(hierarchical boundary register) ip with a mux describe everything within the package file.

Carol – IP providers need to document their ip and provide all the info needed for their ip block.
Francisco – Power domains segments are one issue. Boundary scan segments in the ip are another issue.
Carol – Flags to tell you when the segment is present or not present
Francisco – The order of the segment can be placed anywhere, but within the segment it must be consistent.
Carol – You can pick up an ip block that doesn't support HIGHZ, but all other blocks do. Or SAMPLE. How do we handle this?
CJ – I am a little concerned, there are many permutations and we may not be able to solve them all in the Std. We can use the Std to corral those
cases and push them toward standardizing.
Carol – We should standardize HIGHZ and CLAMP
CJ – Brian can get some numbers on how many BSDL's don't have CLAMP, but we are all over the place.
Carol – This all relates to segmentation. We should call it segmentation mux rather than power mux.
CJ – What's our plan today then? Brainstorming session?
Carol – We should discuss these two.
CJ – We can't leave the Std open ended. We cannot support everything. We need a cut off.
Carol – If we open up segmentation we will need to address the permutations.
Francisco – Is there a schedule of when we need to have things done?
CJ – For summer next year, our draft needs to be wrapped up by end of Dec.
Carol –
CJ – MEC (mandatory editor consideration) needs to be done by end of Dec. MEC can take 30 days and they can ask you to go fix the draft and iterate on it. Carl is starting to get overloaded a little now that he is working.
Roland – With holidays 8-9 weeks this year.
CJ – Yes we need to limit the scope without railroading segmentation. It is going to be tight. I'd like to have it all done by next summer, I don't want it to go into next fall . Let's keep this in mind and cooperate with each other. There may be trade offs we all have to compromise on.

TDR Cells:

CJ presented Figure 9-10 – A self monitoring TDR cell
Carol asked CJ to add a PO wire from UPD cell to Capture cell in the drawing. Carl will revise.
CJ presented Figure 9-11 – A self monitoring and self resetting TDR cell
Bill Bruce – Since this is an odd cell, put in description of where you would want to use this cell.
Carol – Also this violated clock rules, so it would be better to have it drive a clock gate and use TCK as the clock source.
CJ – I'll revisit that and work out the timing diagrams to see if I can improve and clarify this.

Bill – I have a comment on verilog vhdl you use for the TDRs when we have time to talk about it. If you are going to add VHDL and Verilog snippits, then they should be complete. If the drawing is sufficient then no code is needed. If you add the code, then show the complete code with port declarations and so on, so that you don't have to figure things out. Personally I don't think you need the code snippits at all. Are they really needed?
CJ- I think it helps a little.
Carol – Some people are graphically oriented, others like to see code. People's eyes pick up information differently.
Bill – Make the code complete then.
Carol – The snippits could be moved to an annex too?
CJ – Do others want to see the code expanded?
Ken – How much code are you talking about?
Bill – 3 or 4 lines.
Ken – I don't use it.
Dharma – I'd like to see the code snippits.
CJ – Bill I'll ask Carl to complete the code snippits. Francisco has the complete code already.
CJ – Any other issues on clause 9? I'll redo the clocking and timing based on Carol's and Roland's requests.
Francisco – In the event that 1687 doesn't make it through, we still need a 'SIB' feature in 1149.1.
CJ – In our world we are defining it as a cell already done. In 1687 it is ICL code and has many variations.
Bill – Yes, there are many variations.
Carol – We have predefined BSR cells.
Bill – The principle of a SIB is that it is software controlled. An 'n' bit register can become an 'm' bit register. Variable length shift registers described in ICL.
Francisco – We are not looking at it from software in dot 1. It is a TDR between TDI and TDO.
CJ – That is right. In dot 1 it is fixed segments, that are either present or not based on the power mux setting.
Bill – ICL just handles any number of permutations.
CJ – We are predefined.
Bill – OK if predefined it is in 1149.1
CJ – Scan path linkers have existed since 1990.
Francisco – Both teams dot1 and 1687 will have to come to agreements on the overlap between these standards.
CJ – I don't think we have to do anything. Dot1 will help launch 1687.
Bill – I agree with CJ we don't need to worry about the overlap at this point.
CJ – We want dot 1 to have set rules for use at board tests.
CJ – I'm not trying to compete with 1687, we are trying to solve a problem of segmented power domains.
Bill – You have to know the length of the register before EXTEST.

CJ – Agreed. If we add a Boundary Regsiter Segment attribute, they could be assembled in Register Assembly, and a power mux could be used between segments.
Ken – I want the full interconnect on the board. When an IC is there I want to test the full chip.
CJ – Maybe what Ken want's
Carol – Let me give you an example. 4 ethernet ports 2 always powered down.
CJ – Got it. Ken, in one implementation you would
CJ – For board test if you turn on a power domain.
Roland – Power domains for Serdes IP could be common power rails, what granularity for the power_sense are we talking about here when a subset are not used?
Carol – That can be done various ways.
Bill – Why wouldn't you have the logic in there you need for EXTEST, to turn on all the domains for EXTEST?
CJ – This example was for Init-data register, we will have to make some rules for the segmented boundary register.
Bill – PRELOAD and EXTEST are irrevocably linked. Same rules needed to both.
CJ – We want to support board test in system and in the factory.
Ken – For standard mfg board test they all have to be controlled. Today's EXTEST has 20 years of experience behind it. The extra complexity here concerns me. Synthesis and IC test should affect EXTEST at the board level. This is large topic that will likely go beyond Christmas.
Carol – If some ip domains are unpowered and unconnected on a given socket this shouldn't impact board test. Board designer used 2 of 3 ethernet ports for example.
Ken – A power pin would control the unused segment. Power pin strapping.
Bill – If a customer chooses to power down a segment…
CJ – We are over time now. We are discussing how can we make this work, and do we need this? Power domains on chip and within the chip may not be needed for EXTEST, but we need for other scenarios. I'd like to work on how we can make power mux work for Init-data and later look at it for the boundary register.
Francisco- We are looking at 'power aware' concept and need to discuss further.
Wim – Can you send me the power mux slides?

Meeting adjourned: 10:15am MST

Action Items:

- Carol still to present SAMPLE relaxation topic

Next Friday Meeting:

- Next week Friday Oct 7, 2011