1149.10 Discussion

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Introduction

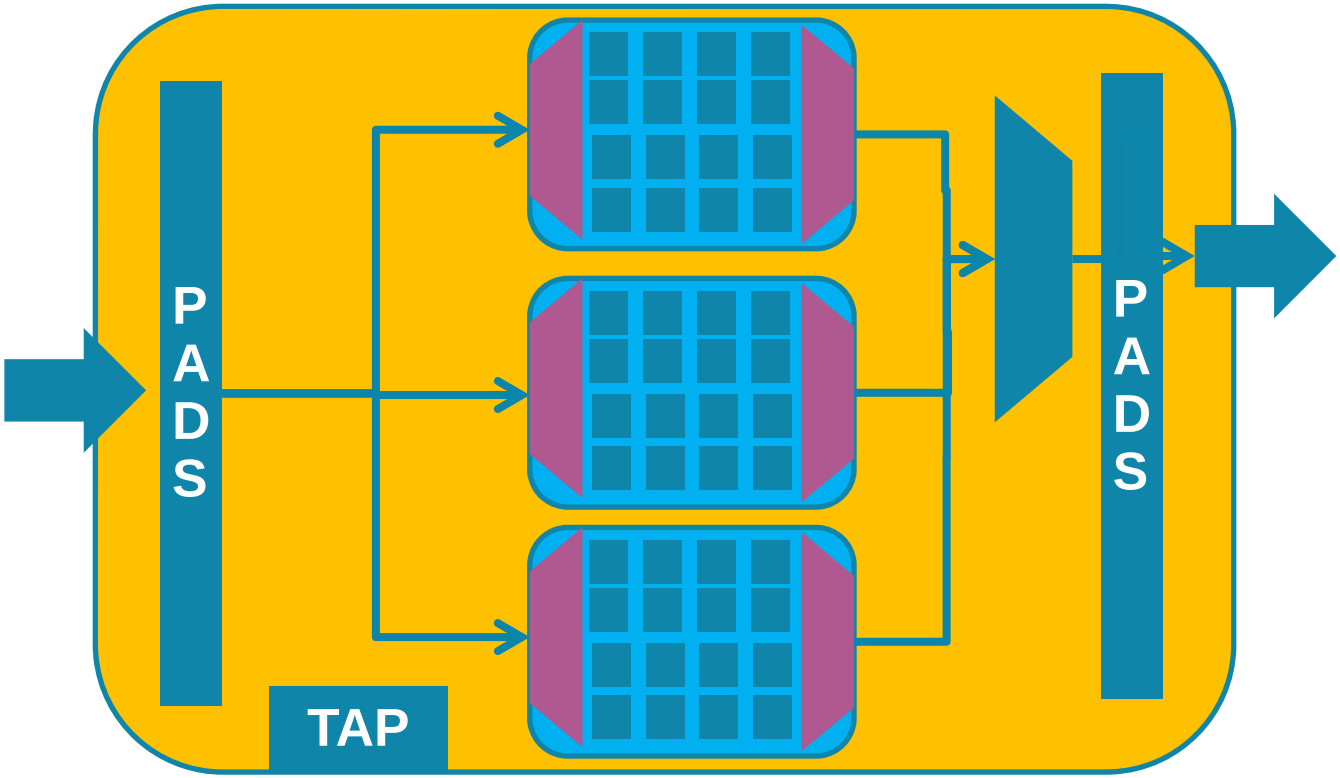
- Describe existing multi-channel scan architecture.
- Map to 1149.10.
- Discussion

Existing Architecture

- Based on ATPG compression:
  - Multiple digital chip pins used as Auxiliary channel input and outputs (typically ~20 but varies per design).
  - 1149.1 TAP used as protocol control (clock, shift, update)
    - Optionally could use dedicated pins but the TAP pins are usually available.
  - Concurrent block testing is supported:
    - Requires unique access to channel inputs (can be broadcast for identical cores).
    - Requires unique access to channel outputs (could optionally include multi-level compression, or multi-pass test).
    - Patterns must be shift aligned (shorter patterns can be shift padded as necessary, or separate clock, shift, updates required).

Existing Architecture

- Digital inputs are broadcast to core channel inputs.
- Core channel outputs are routed out through digital pads.
- Chip TAP provides control signals (clock, shift, update).



Pattern Application

- Tool translates block level patterns to chip level:
  - Channel mapping included in description file.
  - Checks are performed to see that channel resources are available (and are shift length compatible).

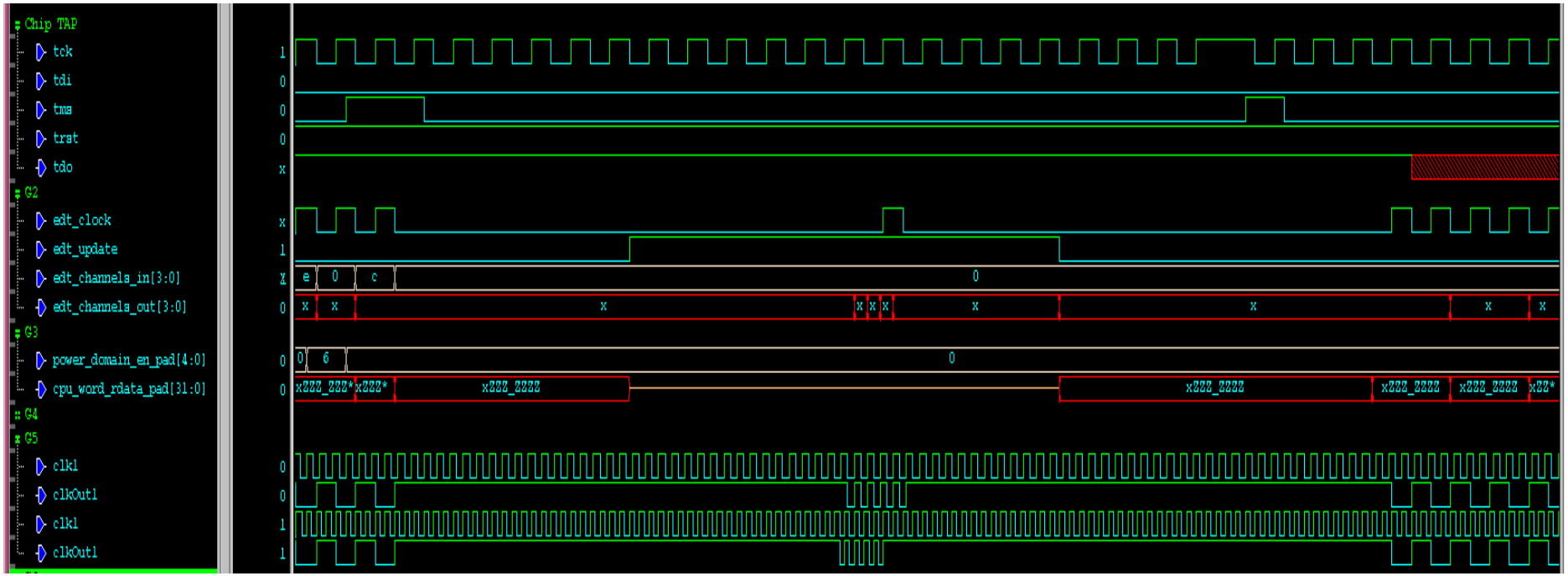
```
scanVerify(atpg_test1) {
    PatternName                     : atpg_test1;
    TckPeriod                       : 10.0ns;
    ClockPeriods {
        mdwr_pad                    : 25.0ns;
        pll_refclk_pad              : 50.0ns;
        core_clock_pad              : 33.333333ns;
    }
    TestStep ( Serial ) {
        Mode                        : compressed_atpg;
        Controller ( I1.ltest ) {
            StilVectorFile          : core1.atpg_vectors_stil;
            StartVector             : 1;
            EndVector               : 2;
        }
        Controller ( I2.ltest ) {
            StilVectorFile          : core1.atpg_vectors_stil;
            StartVector             : 1;
            EndVector               : 2;
        }
        Controller ( I3.ltest ) {
            StilVectorFile          : core2.atpg_vectors_stil;
            StartVector             : 1;
            EndVector               : 2;
        }
    }
}
```

Identical cores

Unique core

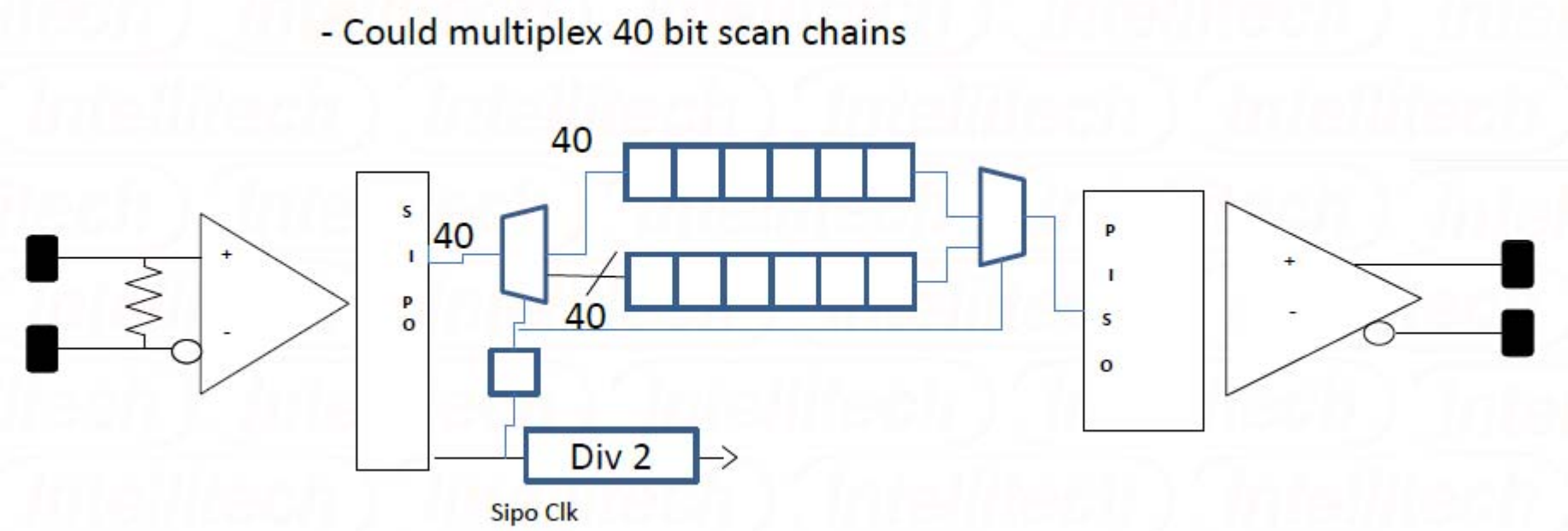
Waveforms

- TAP Controls ATPG compression protocol:
  - Transaction through shift-update-capture states.
- TCK (here) provides the shift clock.
- OCC provides at-speed clocks.



Mapping to 1149.10

- Conceptually similar to earlier discussion:

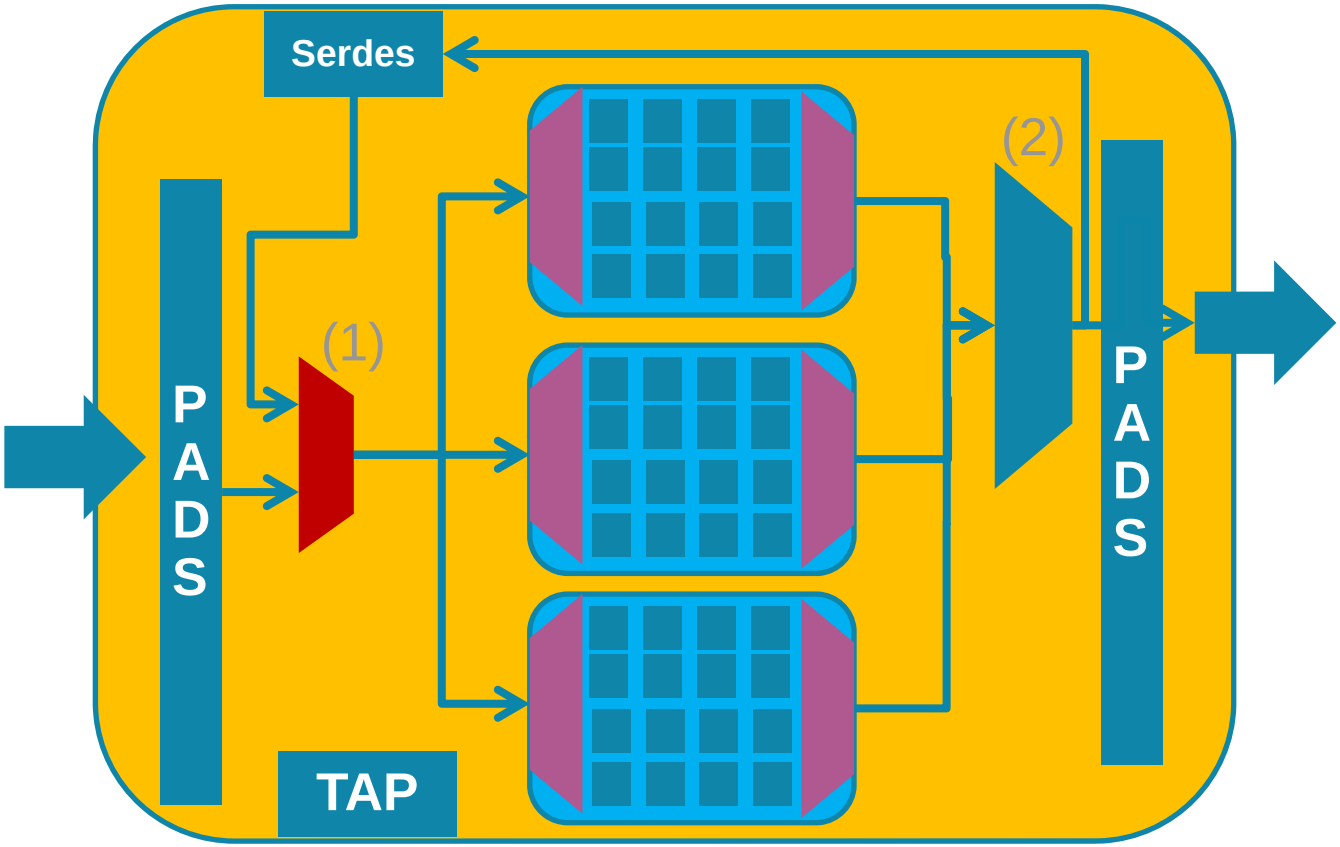


Mapping to 1149.10

(1) Channel inputs are sourced from section of 40 bit word.

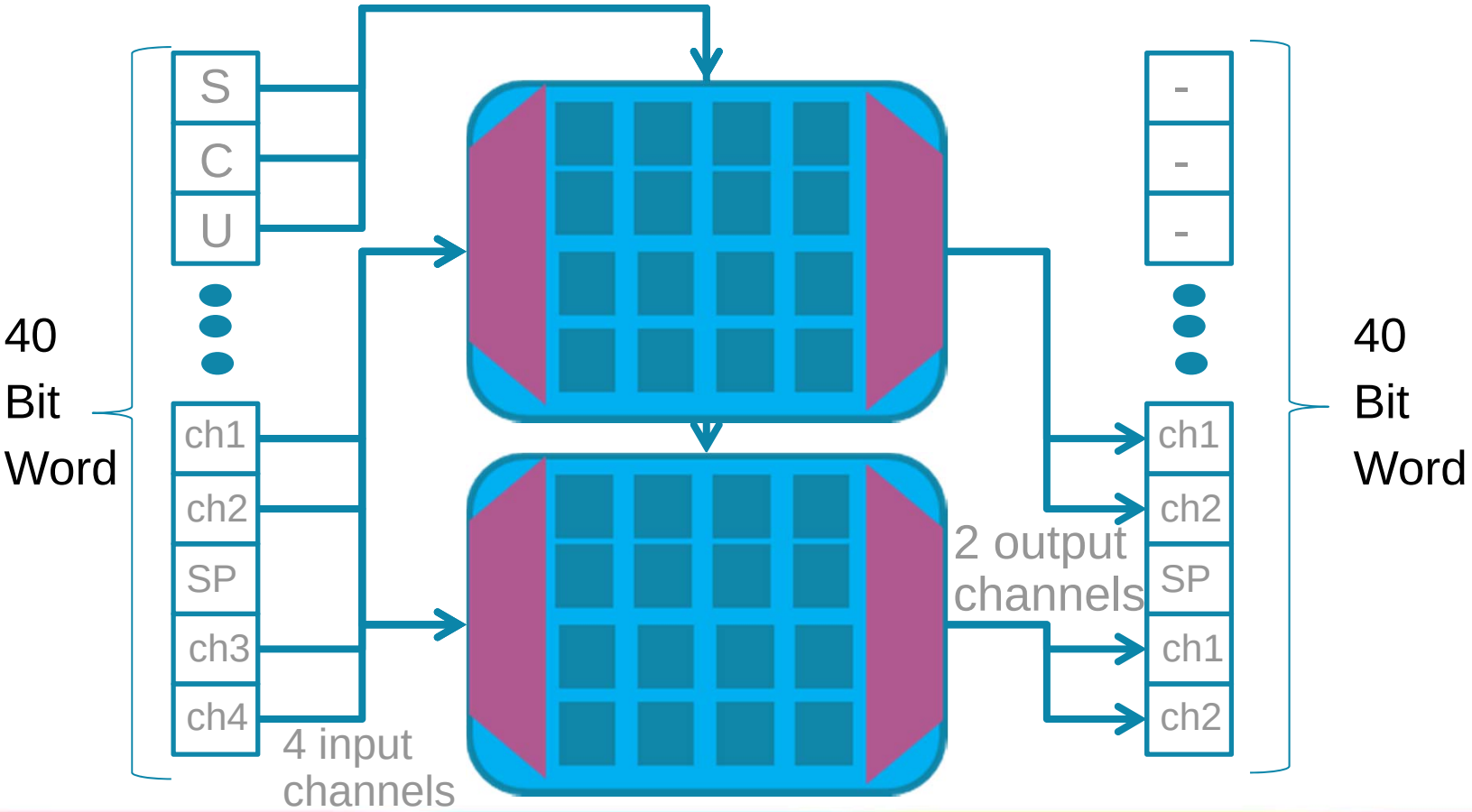
(2) 40 bit serdes word is fed from channel outputs.

(3) Controls (clock, shift, update) sourced from 40 bit serdes word.



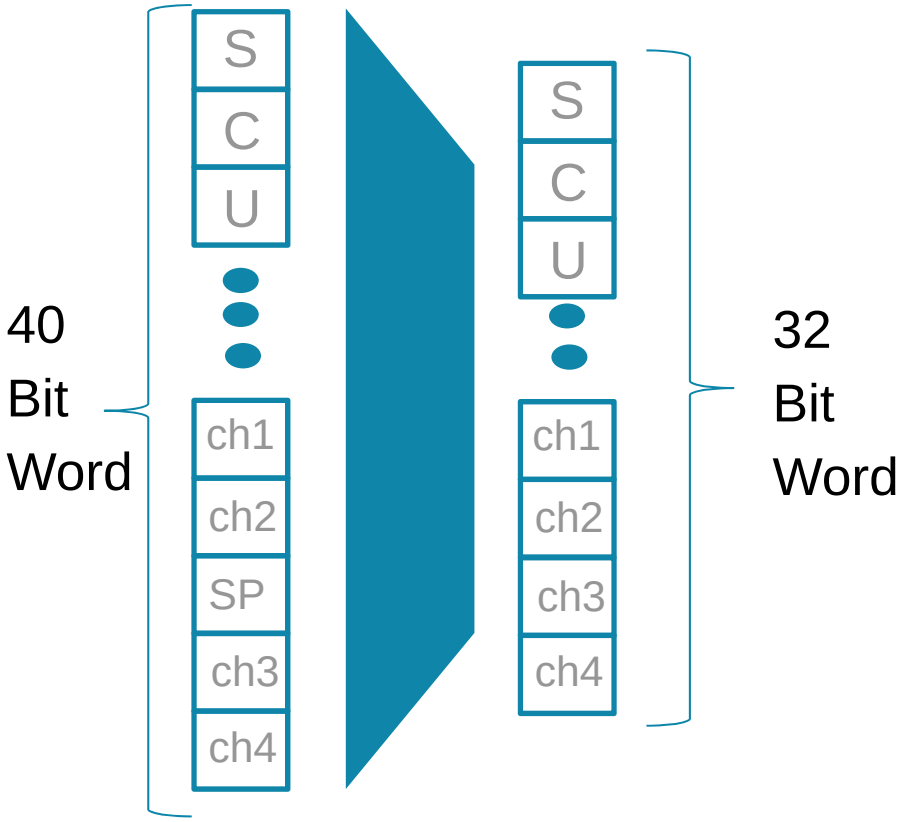
Mapping to 1149.10

- 40 Bit Input Word:
  - Dedicated shift, capture, update.
  - Channel data for scan groups (possibly broadcast).
- 40 Bit output Word:
  - Channel outputs, per scan groups, or multi-level compression.



Data Word Alignment

- 40 Bit Input Word decomposed to 32 usable bits, rest are overhead for clock recovery padding.
- Output 32 to 40 expansion similar.
- Can “gang” multiple words if need more than 32 (-3) parallel channel data.



Summary

- Rarely use 40 channels, usually ~32:
  - Extra bits can be used for shift, update, and capture.
  - Clock recovery (10B8) encoding could be done within unused spare bits interspersed within 40 bit word.
  - Disparity (if necessary) could be encoded as well?
- Often use asymmetric, more inputs 16, less outputs 4. Allows 4 identical cores to be tested concurrently.
- If need more data could “gang” multiple 40 bit words:
  - Requires storage to re- align words.
- Mimics STIL patterns (channel based data on a per cycle basis).