

Date – 06/23/2014

Attendees: CJ Clark, Adam Ley, Bill Tuthill, Bob Gottlieb, Brian Turmelle, Craig Stephan, Dharma Konda, Frans de Jong, Gobinathan Athimolom, Ismed Hartanto, Jon Colburn, Josh Ferry, Mike Ricchetti, Philippe Lebourg, Steve Sunter, Tapan J Chakraborty, Teresa McLaurin,

Absent with Excuse : Saman Adham,

Not Present for $\frac{3}{4}$ of meeting:

Missing: Bill Huott, Carol Pyron, Jim Wilson, Kent Ng, Kevin Gorman, Tom Waayers, Heiko Ehrenburg, Dave Armstrong, Roger Sowada, Dwayne Burek, Gurgen Harutyunyan, Zahi Abuhanmdeh, Marc Hutner,

Agenda:

- 1) Patent Slide
- 2) Review of v22 changes
- 3) New Business
- 4) Adjourn

Meeting Called to order at 11:05 am EDT

Minutes:

Review Patent Slide – Slide Presented to the Group.

Solicited input from anybody who is aware of patents that might read on our standard.

No Response

Steve – signals could have multiple possible meanings

CJ – will be more specific when talking about signals.

Steve – Outside of the group needs to understand the definition of HSTAP and how it is dedicated.

CJ- check out the new wording in the latest revision and see if that is sufficient.

Phillip – new formulation is much clearer.

Steve - Most systems, interfaces between 2 chips talk to each other and RX of one goes to TX of other.

One SERDES is dedicated to talk to one chip. And a different SERDES is dedicated to a 3rd chip so PEDDA to PEDDA need to talk to each other. That seems to be what is missing.

Bob – why would you want that?

Steve – can a PEDDA be connected to multiple SERDES?

Steve – HSTAP hasn't been well defined. Diagram 4-2 doesn't show the HSTAP correctly.

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CJ – the PAR’s description of the HSTAP reuses the High Speed IO. A SERDES can be converted to an HSTAP.

Steve – in dot 1 a TAP is 4 or 5 pins. Just the Pins.

CJ – that is not what it is here.

Steve – it isn’t clear here.

CJ – If we need to fix it to make it more clear than open to suggestion.

Steve- What do you exactly mean by the HSTAP?

Philippe – maybe we should refer to original meaning. HSTAP is for high speed test access ports. It doesn’t define a port but an interface.

Steve- so if that is the way the group wants to define it, that is fine but we will need to make some corrections. It is the port and not any circuitry.

Steve – the word Port is defined in 1149.1 and we need to define Port for 1149.10. Need to be able to agree on the most basic terms of the standard.

Tapan – primary interface is not a port only. It has some circuitry with it.

CJ – never been any discussion with pins going into PEDDA. Interface has been everything into in the PEDDA

Bob – not mandating it is the SERDES. The interface between the pins and the PEDDA is not being standardized. It doesn’t matter what is there. We are not standardizing what that logic is.

Steve – includes the Serial to parallel and parallel conversion?

CJ – it may or may not. It depends on implantation.

Steve –Feels that this point is not resolved.

Bob – would like to go back to the discussion about splitting the PEDDA or would you need dedicated interfaces.

CJ – would normally not daisy chain SERDES so that figure might not be the best example. Opportunity to putting your HSIO into a HSTAP by sending a control character.

CJ – could daisy chain in a stack of die or chips though.

Steve – PEDDA could have way to take information in on one SERDES port and send it out on another SERDES port

CJ – that is what we are showing.

Steve – no you are showing the same SERDES.

CJ – This is just a block diagram. Doesn’t need to be the same RX/TX pair.

Steve – should convey the use in a practical situation.

CJ – so the comment was that we brought it without introducing it.

Bob – realistically you are not going to put the input of the chain in a different part of the output and expect it to work.

CJ – don’t need to solve all the applications. Need to provide the frame work.

Bob – need to have solutions that we believe work for the intended uses. Something we struggle with connecting high speed devices.

CJ – agree with that.

CJ – Output of one HSTAP can be connected with input of another because we have Target ID. That is the important part of the figure. Engineering is more involved. Here we are showing what the architecture saying that output of one HSTAP can be connected to the input of another.

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Steve- never seen a tick mark followed by Asterisk.

CJ – it has been updated. RESET10 instead of RESET’

CJ – not hearing objection.

CJ – some small changes. Some concern about what a control character is so that was defined better.

Steve – how did you define “control character”?

CJ – any of the special symbols in 8b/10b

Steve – in the concept of 8b/10 it is well understood. So you are meaning it to be the same as 8b/10b

Philippe – does that mean that 8b/10b is mandated?

CJ – no. 8b/10b is an example.

Tapan – don’t understand why you put 10 on RESET10.

CJ – it was Steve’s suggestion to use instead of an ‘

Steve – the tick was hard to read. The Alphanumeric was easier to read.

CJ –The reset duration is something the designer is going to manage.

Steve – if the chip has a requirement. You can’t just issue the command and go to the next command. The chip might need some time. Where does that get documented?

CJ – in PDL.

Steve- it should be documented somewhere

CJ – section isn’t dedicated to PDL and would like to put it in the PDL section.

CJ – in the PDL you would have to put in the WAITs that are necessary.

Steve – table 6-3, does this show a bunch of examples.

CJ – showing a packet transmitted. Left it because it is a useful tool for the diagram below. Config packet is shown. And this is the bites that are needed to implement that packet.

Steve – table 6-3 is showing the bytes that are in table 6-5?

CJ – it might be that it flips from one page to the other it may not be that clear. Shows how that RESET is asserted. Want to make sure people know how the packet is formed.

Steve- relying on the reader to look at each byte and understand what is going on.

CJ – if you don’t find it useful than you don’t need to use it. Wanted to show the SOP and EOP being integrated into a packet.

Philippe – Responded to in email. ICSU is an acronym since it stands for Idle Capture Shift Update.

CJ- Ok. Copied definition and placed in Acronym section.

No Call for New Business

No new business

Please use reflector to review what is in the Draft.

Please send comments to reflector.

Anything that needs to be fixed. Or comments on State Diagram.

Motion to Adjourn: Philippe
Seconded: Bob
Meeting adjourned: 12:00 pm EDT

Next Meeting:
June 30th, 2014 11:00am

Motion Summary

0 motions made

Action Items

~~*Bill Tuthill – 10-21-2013 – Add minutes and Attendance spreadsheet to the website.*~~
~~*CJ – 11-11-2013 – Reach out to ATE industry and Probe Industry to get update on future of ATE equipment to see which data speeds and protocols they are heading towards.*~~

Philippe – Look into alternative method to create control information (pause, start, terminate, etc.) rather than using K characters in packet.

Bob – create a case study to show use of Attributes

Frans – will start some block diagrams of a simple use case to help illustrate the current architecture

~~*Dwayne – present to the group his ideas for a simplified scheme – Direct Interface.*~~

NOTES:

1149.10 working group website - <http://grouper.ieee.org/groups/1149/10/>

Here is the WebEx conference link.

<https://meetings.webex.com/collabs/meetings/join?uuid=MAG12PB7HN5W24AM2EOKIOM9KS-KERT>

You can use VOIP on your computer or dial-in using the phone number below.

Audio Connection

+1-415-655-0001

Access code: 194 196 960