Date – 12/01/2014
Attendees: CJ Clark, Adam Ley, Bill Tuthill, Bob Gottlieb, Brian Turmelle, Craig Stephan, Dharma Konda, Frans de Jong, Jon Colburn, Marc Hutner, Steve Sunter, Tapan J Chakraborty,

Absent with Excuse:
Not Present for ¾ of meeting:

Missing: Bill Huott, Carol Pyron, Jim Wilson, Kent Ng, Kevin Gorman, Tom Wayers, Heiko Ehrenburg, Dave Armstrong, Roger Sowada, Dwayne Burek, Zahi Abuhanmdeh, Mike Ricchetti, Saman Adham, Gurgen Harutyunyan,
Teresa McLaurin, Philippe Lebourg,
Josh Ferry,
Gobinathan Athimolom, Ismed Hartanto,

Agenda:

1) Patent Slide
2) Discussion of Clause 8
3) New Business
4) Adjourn

Meeting Called to order at 11:08 am EST

Minutes:
Review Patent Slide – Slide Presented to the Group.
Solicited input from anybody who is aware of patents that might read on our standard.
Adam Ley Notes (sent on reflector)
PN, TTL, AN
7348796, METHOD AND SYSTEM FOR NETWORK-ON-CHIP AND OTHER INTEGRATED CIRCUIT ARCHITECTURES, DAFCA INC.

No other responses noted.

Discussion of Clause 8
Cleaned up Rule b)
Cleaned up wording for BOND packet per Tapan's discussion
added note in e) to add clarification
updated example section
Craig sent some updates over reflector.
Frans – note on e) says "until". What is next?
Round robin in this case is actively controlled?
CJ – Alignment character.

CJ – would like to vote this section up or down next week.

CJ made some Clause 7 tweaks
Syntax Min_byte count and max_byte_count added as integers
Fixed rule m) so lane Zero is the first lane and must have at least 1 lane
Added rule for min and max byte count
7.7 BSDL package for high speed JTAG
Defines a package file for BSDL "STD_1149_10_201x" - x to be updated when standard is voted in

PLD section 9 needs to be written for compliance
Adding a Compliance Verification section (section 9.10)

Tapan – what needs to be added to a parser?
CJ – all the grammar that is in Section 7
If you don't support the standard than you could add BSDL extensions

New Business
Steve – Since this is the first standard proposed to share the DOT1 instruction register. Is there any chance we are introducing a new aspect where DOT1 writes something the IR and the HSTAP writes something to IR and DOT1 now has no idea what is in the IR now Is there a chance something will get screwed up?

Same thing with the Boundary Scan register and you clamp or unclamp something and the DOT1 TAP loses knowledge of what is going on in the chip

Bob- do we ever thing that the two agents are not aware of each other? Or are they always going to be aware of each other and take each other into account.
Steve – at the board level, there are a lot of dot1 agents.
Bob – if the two taps can't be aware of each other maybe we need something to put the DOT1 TAP into a certain state.
CJ – your use model seems a little different than what we were envisioning.
Where you are doing something with the 1149.1 TAP and then going into the HSTAP and come back to DOT1
No guaranteed to have IR register same after the HSTAP. No intention to have a back and forth between TAPS occurring. Would need to reconfigure the registers when going back to the DOT1 TAP
CJ – if you have a proposal to sync these things up we can go over them.
Steve – just trying to see if there are any issues going from one controller to another.
Bob – not worried about handing over the IR. No expectations that any registers have the same state when going back and forth.
How does that transition happen from Dot10 to Dot1?
CJ – state diagram shows how to get out of the HSTAP and PEDDA
Bob – do we always go back to mission mode when we want the DOT1 to be used?
CJ – yes. In the figures. Power off/ reset/ using the tap to run the sequence.
Bob – but if we want to use DOT1 we should be in mission mode?

CJ – yes you need to get the HSTAP out of being the HSTAP
Bob – should say that we want to use 1149.1 we should say that 1149.10 is disabled.
CJ – Go back to section 4 and see what is missing.
There is no way from the HSTAP and PEDDA to change back to DOT1.
You need to go in the DOT1 Interface and disable the 1149.10
Bob – DOT1 shouldn't be available while DOT10 is enabled?
CJ – The TAP is still there and still function. You can't scan a register because we are in DOT10 mode which turns the mux to the PEDDA. Nothing would go through the DOT1 interface. It is being blocked by the 1149.10 enable.
Bob – we are not going to put all the scan chains to the HSTAP. We shouldn't be able to scan these non HighSpeed registers.
CJ- No rule from preventing you from doing it, but would be a lot of challenges to doing this.
Marc – in the standard you should say that you are allowed to load data and touch the TAP controller at the same time. But add a note that there are some problems that come along with this.
Steve – if you have the IR has a mux you can't do anything with the DOT1 interface.
Marc- that is what we should take away so you can still touch the DOT1 interface
CJ- in Bob's example he might not hook the IR register to this at all.
Bob – single instruction register and we are bifurcating what we can do two different 1149.x things at the same time? Those two things don't make sense together.
CJ – Its been true since the beginning. Once you throw the mux you can't do anything with 1149.1
Nothing in the standard saying you can't scan the instruction register. Optional to control the IR by the mux.
No requirement to include IR in PEDDA.
Just use the HighSpeed interface to load data into the internal scan chain.
People will come up with their own solutions. Don't want to add restrictions.
Steve – ICU byte if set to instruction could be ignored.
CJ – yes for that design of the PEDDA it can be ignored.
Scan Channel association tells me what is accessible
Steve – should make it clear that all the registers are optional including the IR
CJ – ok.. Can go back into the document and see what we have wrong.
Tapan – what benefits do I have to access these registers from DOT10?
CJ – benefits access to DOT1 instruments. Voltage and Temperature monitors can be monitored while loading test patterns through the High Speed interface.
But in the first steps in DOT10 many people have mentioned that they don't want to interface into their DOT1 registers. And you are free to do that.
Steve – What if there is DOT1 interface. Do we still need an IR?
CJ – don't need to.
Steve – if you do provide access to IR than there should some clarification on the proper handoff
CJ – We can add some clarification into the document. Section in Clause 4 that discusses enabling and disabling the HSTAP.
CJ – Don't want to create rules where rules don't need to be

Send any New Business requests to the reflector

Please use reflector to review what is in the latest version of the draft. Please send any comments on the new material to the reflector. This will let us get a start on the material before the meeting. Please include anything that needs to be updated or anything you would like discussed

Motion to Adjourn: Steve
Seconded: Frans
Meeting adjourned: 12:03pm EST

Next Meeting:
Dec 8th, 2014 11:00am

Motion Summary
0 motions made

Action Items
~~Bill Tuthill – 10-21-2013 -Add minutes and Attendance spreadsheet to the website.~~
~~CJ 11-11-2013 Reach out to ATE industry and Probe Industry to get update on future of ATE equipment to see which data speeds and protocols they are heading towards.~~
Philippe – Look into alternative method to create control information (pause, start, terminate, etc.) rather than using K characters in packet.
Bob – create a case study to show use of Attributes
Frans – will start some block diagrams of a simple use case to help illustrate the current architecture
~~Dwayne – present to the group his ideas for a simplified scheme – Direct Interface.~~
~~Adam – invite someone from IEEE to speak on IEEE benefits of standardization at WG meeting~~

Patent notes
Adam Ley 12/1/2014

PN, TTL, AN
7348796, METHOD AND SYSTEM FOR NETWORK-ON-CHIP AND OTHER INTEGRATED CIRCUIT ARCHITECTURES, DAFCA INC.

Steve Sunter 11/17/2014

1. US 7610532 “Serializer/de-serializer bus controller interface” Avago, granted 2009
2. US 7739567 “Utilizing serializer-deserializer transmit and receive pads for parallel scan test data” Avago, granted 2010
3. US 8543876 “Method and apparatus for serial scan test data delivery” Altera, granted 2014

NOTES:

1149.10 working group website - http://grouper.ieee.org/groups/1149/10/

Here is the WebEx conference link.

https://meetings.webex.com/collabs/meetings/join?uuid=MAG12PB7HN5W24AM2EOKIOM9KS-KERT

You can use VOIP on your computer or dial-in using the phone number below.
Audio Connection
+1-415-655-0001
Access code: 194 196 960