IEEE 1149.4 Mixed-Signal Test Bus Working Group Meeting Minutes

for

May, 23rd **2005**

9:00AM-11:00AM

Meeting Agenda:

Time	Topic	Responsibility
9:00 AM	1. Introduction	Bambang Suparjo
9:05-11:00 AM	1. Review on MST Kitchen Sink Proposal. 2. Next Actions.	Adam Ley
11:00 AM	Summary and Adjourn	Bambang Suparjo

Meeting Attendees:

Name	Company
Adam Ley	Asset-Intertech
Keith Lofstrom	Keith Lofstrom Integrated Circuits
Ken Parker	Agilent Technologies
Heiko Ehrenberg	Goepel Electronics LLC
Bambang Suparjo	Mentor Graphics

1. Introduction

Bambang welcomed the group and members to the meeting and presented the Meeting Minutes April 5th 2005. Adam Ley pointed out an issue regarding the instruction opcode in minute 2.1 (b). He will discuss this issue off-line with Adam Cron.

2. Review of MST Kitchen Sink Proposal

Adam Ley presented the MST Kitchen Sink Proposal. The detail discussions are reported below and the complete proposal is shown in Appendix A.

2.1 Attribute PORT_GROUPING

He started the presentation with the explanation on PORT_GROUPING attribute as shown below:

```
-- grouped port identification, as per 1149.1
-- = required for digital differentials
attribute PORT_GROUPING of Kitchen_Sink_2_2 : entity is
     "Differential_Voltage ((D1, D1N),(X1,X1N)),"&
     "Differential_Current ((D2, D2N),(X2,X2N))";
```

The purpose of including this attribute is to describe the analog differential pair. He requested opinion from the group if this attribute is required in 1149.4. Ken suggested that the attribute should be included so that the tool can understand the differential pair description.

Adam Ley added, by including the attribute, the 1149.1 tool has the opportunity to apply differential test scheme in digital interconnect since each pin has its own boundary cell.

2.2 Attribute INSTRUCTION_OPCODE

```
attribute INSTRUCTION_OPCODE of Kitchen_Sink_2_2 : entity is
  -- mandatory instructions, as per 1149.1
     "EXTEST  (1000), " &
     "PRELOAD (0010), " &
     "SAMPLE  (0010), " &
     "BYPASS  (0111), " &
  -- mandatory instruction, as per 1149.4
  -- = opcode may have any value except all ones
  -- = opcode value all zeros is not recommended (as per 1149.1)
     "PROBE   (1011), " &
  -- optional instructions, as per 1149.1
     "CLAMP   (0100), " &
     "HIGHZ   (1101), " &
     "INTEST  (1110), " &
     "IDCODE  (0001)";
```

The group agreed with the proposed instruction opcode. Other optional instructions can also be added in the list.

2.3 Attribute IDCODE_REGISTER

```
attribute IDCODE_REGISTER of Kitchen_Sink_2_2 : entity is
     "XXXX" &              -- version
     "0000000000000000" & -- part number
     "10101010101" &       -- manufacturer id
     "1";
```

Adam Ley was referring to IEEE 1532 standard and found the proposed manufacturing ID is not used.

2.4 Attribute BOUNDARY_REGISTER

2.4.1 Digital Differential Pins

```
  -- following cells (6) are for the digital differential pins
  -- num cell port function safe [ccell disval rslt]
     "2  (BC_1,   D1, input,        x), " &
     "3  (BC_1,  D1N, input,        x), " &
     "4  (BC_1,    *, internal,     x), " &  -- D1:D1N SE
     "5  (BC_1,   D2, input,        x), " &
     "6  (BC_1,  D2N, input,        x), " &
     "7  (BC_4,    *, internal,     x), " &  -- D2:D2N SE
```

D1 and D1N are the differential pair that associated to the single ended point at cell 4. The setting on each cell is following the 1149.1 requirements. BC_1 cell type can also be used at cell 7.

2.4.2 TBIC Base Controls

```
-- following cells (4) are TBIC  base controls
-- num cell port function safe [ccell disval rslt]
   "8  (BC_1,    *, internal,     0), " &           -- Ca
   "9  (BC_1,    *, control,      0), " &           -- Co
   "10 (BC_7,  AT1, bidir,        0,  9, 0, Z), " & -- D1
   "11 (BC_7,  AT2, bidir,        0,  9, 0, Z), " & -- D2
```

Since cell 9 is used to control the bidirectional cells (cells 10 and 11), the save value of the cell needs to be set to 0. For the internal cell (cell 8), by setting the save value to 0, it will prevent calibration mode from being invoked during conventional 1149.1 EXTEST operation.

Setting the save values of cell 10 and cell 11 to 0 satisfied the TBIC switching patterns for conventional EXTEST mode and extended interconnect test applications. The relevant patterns are P1, P2 and P3 as shown in Table 1 of the 1149.4 standard. While this setting is perfectly valid for 1149.4 applications, the save value determination should also consider applications in 1149.1 context. As an example, in order to apply extended interconnect testing, test data (either 0 or 1) can be set at cell 10 and cell 11, but if the cells do not involve in any application, they should be set to 0. Similarly, to apply conventional 1149.1 EXTEST, cell 9 needs to be set to 1 in order to allow cells 10 and 11 applying 0 and 1 states at their associated pins.

2.4.3 TBICN Base Controls

```
-- following cells (4) are TBICN base controls
-- num cell port function safe [ccell disval rslt]
   "14 (BC_1,    *, internal,     0), " &           -- Ca
   "15 (BC_1,    *, control,      0), " &           -- Co
   "16 (BC_7, AT1N, bidir,        0, 15, 0, Z), " & -- D1
   "17 (BC_7, AT2N, bidir,        0, 15, 0, Z), " & -- D2
```

TBICN is needed for fully differential test application. In Figure 27 of the 1149.4 standard, the TBIC inverting portion name is TBIC(N). However the prentices cannot be included in BSDL identifier, and therefore they need to be removed.

2.4.4 TBIC Extension Controls

```
-- following cells (4) are TBIC  extension controls
-- num cell port function safe
   "12 (BC_1,    *, internal,     0), " &           -- D1
   "13 (BC_1,    *, internal,     0), " &           -- D2

-- following cells (2) are TBIC  extension controls
-- num cell port function safe
   "18 (BC_1,    *, internal,     0), " &           -- D1
   "19 (BC_1,    *, internal,     0), " &           -- D2
```

Heiko asked are cells 12 and 13, and cells 18 and 19 duplicated. Adam Ley said, they are not duplicated, where in this example there are additional internal test buses as shown in attribute MST_TBIC_Register.

```
-- TBIC  register, as per 1149.4
-- = ref tables 1 and 2
attribute MST_TBIC_Register  of Kitchen_Sink_2_2 : entity is
  -- Ca_num Co_num
     " 8,  9 : " &
  -- { partition_name D1_num D2_num}
     " IATB0 (10, 11), " &
     " IATB1 (12, 13), " &
     " IATB2 (18, 19)";
```

Adam Ley added, cells 20 and 21 are for the extension on the N-side, to control additional AT1N and AT2N test buses. The comment on cell 21 should be D2, not D1.

```
  -- following cells (2) are TBICN extension controls
  -- num cell port function safe
     "20 (BC_1,    *, internal,     0), " &          -- D1
     "21 (BC_1,    *, internal,     0), " &          -- D1
      .
      .
-- TBICN register, as per 1149.4
-- = ref tables 1 and 2
attribute MST_TBICN_Register of Kitchen_Sink_2_2 : entity is
  -- Ca_num Co_num
     "14, 15 : " &
  -- {Npartition_name D1_num D2_num}
     "NIATB1 (16, 17), " &
     "NIATB2 (20, 21)";
```

2.4.5 Cells controlling ABMs

```
  -- following cells (4) control the analog signal W
  -- num cell port function safe [ccell disval rslt]
     "22 (BC_1,    *, control,      0), " &          -- C
     "23 (BC_7,    W, bidir,        x, 22, 0, Z), " & -- D
     "24 (BC_1,    *, internal,     0), " &          -- B1
     "25 (BC_1,    *, internal,     0), " &          -- B2
```

Adam Ley will review the switching patterns for ABM in order to set the appropriate save value on the bidirectional cell, in this case is cell 23 for pin W. The save value setting is also applied to the other bidirectional cells in other ABMs i.e. cells 27, 31, 35, 39 and 43 in the proposal. The 1149.1 does not have to know/care the special conditions in analog differential measurement mode.

2.5 ATAP and ATAPN port identification

The AT1, AT2, AT1N and AT2N ports can be identified by referring to the attributes shown below:

```
-- ATAP  port identification, as per 1149.4
attribute MST_ATAP_AT1  of Kitchen_Sink_2_2 : entity is "AT1";
attribute MST_ATAP_AT2  of Kitchen_Sink_2_2 : entity is "AT2";

-- ATAPN port identification, as per 1149.4
-- = only required for optional differential ATAP
attribute MST_ATAP_AT1N of Kitchen_Sink_2_2 : entity is "AT1N";
attribute MST_ATAP_AT2N of Kitchen_Sink_2_2 : entity is "AT2N";
```

2.6 Attribute MST_TBIC_Register

```
-- TBIC  register, as per 1149.4
-- = ref tables 1 and 2
attribute MST_TBIC_Register  of Kitchen_Sink_2_2 : entity is
  -- Ca_num Co_num
     " 8,  9 : " &
  -- { partition_name D1_num D2_num}
     " IATB0 (10, 11), " &
     " IATB1 (12, 13), " &
     " IATB2 (18, 19)";

-- TBICN register, as per 1149.4
-- = ref tables 1 and 2
attribute MST_TBICN_Register of Kitchen_Sink_2_2 : entity is
  -- Ca_num Co_num
     "14, 15 : " &
  -- {Npartition_name D1_num D2_num}
     "NIATB1 (16, 17), " &
     "NIATB2 (20, 21)";
```

The TBIC register contains the cells' numbers of the calibrate cell Ca, control cell Co, and the pair of data cells D1 and D2 for every internal test bus partition that exist. Ken asked is IATB0 arbitrary name. Adam Ley said the partition name is arbitrary name, not using reserve word.

2.7 Attribute MST_Diff_Pins_Table

```
attribute MST_ABM_Pins_Table of Kitchen_Sink_2_2 : entity is
  -- ABMs, as per 1149.4 = ref tables 6, 7, and 8
  -- port partition_name C_num D_num B1_num B2_num
     "W   (  IATB0: 22, 23, 24, 25 ), " &
     "Y   (  IATB0: 26, 27, 28, 29 ), " &
     "X1  (  IATB1: 30, 31, 32, 33 ), " &
     "X1N ( NIATB1: 34, 35, 36, 37 ), " &
     "X2  (  IATB2: 38, 39, 40, 41 ), " &
     "X2N ( NIATB2: 42, 43, 44, 45 )";
```

This attribute contains, port name which is associated with its partition and the ABM cells' numbers. The partition will provide information on which TBIC cell to use and the list of four cells will provide information on which ABM cell to use for a given port.

2.8 Attribute MST_Diff_Pins_Table

```
attribute MST_Diff_Pins_Table of Kitchen_Sink_2_2 : entity is
  -- DBMs at single-ended side of differential drivers/receivers
  -- representative_port associated_port num
     "D1 : D1N ( 4), " &
     "D2 : D2N ( 7)";
```

In order for the 1149.4 description to be complete, not only we need to know which cell associated with which port but need to know which cell functioning as a driver and which cell as a receiver. Ken asked are D1 and DIN are the receiver differential pair and have a single ended point at cell 4. Adam Ley replied that is correct. Adam Ley added, the example is too primitive and needs to be more sophisticated. The pin order is also defined the polarity i.e. D1 is positive and D1N is negative.

2.9 General Comment

Keith was referring to Table 6 and Table 8 of the 1149.4 standard and relate them to the save value question that has been raised previously on cells 31, 35, 39 and 43. If the pattern becomes 0100 ($C/D/B_1/B_2$) which is P4, then the pin will be connected to V_G, which is not a save condition. Adam Ley went through the tables and suggested patterns P0 (0000 – completely isolated), P8 (1000 – connected to V_L) and P12 (1100 – connected to V_H) are the required patterns. If the D bit is modulated from P0 (0000), it will become P4 (0100) which is needs to be avoided. If the D bit is modulated from P8 (1000), it will become P12 (1100) which is needed. Therefore the save value should be 0 but Adam Ley will review further this issue.

2.10 Issue on internal cells

Adam Ley brought back the internal cells issue that Keith has raised in previous meeting. In brief, Keith might be interested to have a limited means to describe the internal cells in ABSDL. Adam Ley asked Keith on which patterns would be valid at ABM that wired to a linkage pin. Keith answered that he would like to avoid the V_{DD} pin from being connected to V_L. Keith will do research to identify the patterns that are valid for this case.

2.11 Status of ABSDL development

Bambang requested opinion from the group on the Straw_Dog status. Adam Ley answered that the Straw_Dog_2.1 version required to be updated and that is why he introduced Kitchen_Sink, trying to flesh out the issues. Then if that issues stable, take the Kitchen_Sink and trim it down to a Straw_Dog that shows a minimal subset. The next stage of the work is determining semantic rules related to 1149.4. Heiko volunteered to prepare the first draft of the semantic rules.

2.12 Participation

Keith raised a concern on the number of members participate in the meeting which has been declining.

3. Next Action

3.1 Adam Ley will review the switching patterns in order to set the appropriate save value on the bidirectional cell in the ABM (refer to minutes 2.4.5 and 2.9).

3.2 Keith will do research to identify the patterns that are valid at ABM that wired to a linkage pin (refer to minute 2.10).

3.3 Heiko will prepare the first draft of semantic rules related to 1149.4 (refer to minute 2.11).

4. Summary and Adjourn

Bambang summarized the meeting and the teleconference was adjourned at 11:00 AM.

Appendix A – MST Kitchen Sink Proposal

```
-- 2005/05/20
-- MST Kitchen Sink version 2_2
-- BSDL description of an example 1149.4 device
-- This is an 1149.1-compatible BSDL that encodes 1149.4 features.
-- This remains suitable for use with conventional 1149.1 tools.
-- (such tools may/ will simply ignore the elements that support
--   features pertaining only to 1149.4)


entity Kitchen_Sink_2_2 is
generic (PHYSICAL_PIN_MAP : string := "dip24");

port(

  -- TAP pins, as per 1149.1
     TCK, TDI, TMS: in bit;
     TDO: out bit;

  -- ATAP pins, as per 1149.4
  -- = required to be inout (bidirectional)
     AT1, AT2: inout bit;

  -- ATAPN pins, as per 1149.4
  -- = only required for optional differential ATAP
  -- = required to be inout (bidirectional)
     AT1N, AT2N: inout bit;

  -- digital pins, as per 1149.1
  -- = type/ direction not restricted
     A, B: in bit;

  -- digital differential pins, as per 1149.1
  -- = type/ direction not restricted
     D1, D1N: in bit;
     D2, D2N: in bit;

  -- analog pins, as per 1149.4
  -- = required to be inout (bidirectional)
     W, Y: inout bit;

  -- analog differential pins, as per 1149.4
  -- = required to be inout (bidirectional)
     X1, X1N : inout bit;
     X2, X2N : inout bit;

  -- linkage pins, as per 1149.1
     NC1, NC13: linkage bit;
     GND, VCC: linkage bit);

-- standard use statement, as per 1149.1
use STD_1149_1_2001.all; -- Get Std 1149.1-2001 attrs and defns

-- optional use statement, as per 1149.1
-- = standard use statement, as per 1149.4
use STD_1149_4_2005.all; -- Get MST attributes and definitions
```

```
-- component conformance, as per 1149.1
attribute COMPONENT_CONFORMANCE of Kitchen_Sink_2_2 : entity is
     "STD_1149_1_2001";

attribute PIN_MAP of Kitchen_Sink_2_2 : entity is PHYSICAL_PIN_MAP;

constant dip24 : PIN_MAP_STRING :=
  --       -----------
  --  NC1  | 1    24 | VCC
  --    A  | 2    23 | W
  --    B  | 3    22 | Y
  --   D1  | 4    21 | X1
  --  D1N  | 5    20 | X1N
  --  D2N  | 6    19 | X2N
  --   D2  | 7    18 | X2
  --  AT1  | 8    17 | AT2
  -- AT1N  | 9    16 | AT2N
  --  TDI  | 10   15 | TDO
  --  TCK  | 11   14 | TMS
  --  GND  | 12   13 | NC13
  --       -----------
     "TCK:11, TDI:10, TMS:14, " &
     "TDO:15, " &
     "AT1:8, AT2:17, " &
     "AT1N:9, AT2N:16, " &
     "A:2, B:3, " &
     "D1:4, D1N:5, " &
     "D2:7, D2N:6, " &
     "W:23, Y:22, " &
     "X1:21, X1N:20, " &
     "X2:18, X2N:19, " &
     "NC1:1, NC13:13, " &
     "GND:12, VCC:24";

-- grouped port identification, as per 1149.1
-- = required for digital differentials
attribute PORT_GROUPING of Kitchen_Sink_2_2 : entity is
     "Differential_Voltage ((D1, D1N),(X1,X1N)),"&
     "Differential_Current ((D2, D2N),(X2,X2N))";

attribute TAP_SCAN_CLOCK of TCK : signal is (20.0e6, BOTH);
attribute TAP_SCAN_MODE of TMS : signal is true;
attribute TAP_SCAN_IN of TDI : signal is true;
attribute TAP_SCAN_OUT of TDO : signal is true;

attribute INSTRUCTION_LENGTH of Kitchen_Sink_2_2 : entity is 4;

attribute INSTRUCTION_OPCODE of Kitchen_Sink_2_2 : entity is
  -- mandatory instructions, as per 1149.1
     "EXTEST  (1000), " &
     "PRELOAD (0010), " &
     "SAMPLE  (0010), " &
     "BYPASS  (0111), " &
  -- mandatory instruction, as per 1149.4
  -- = opcode may have any value except all ones
  -- = opcode value all zeros is not recommended (as per 1149.1)
     "PROBE   (1011), " &
  -- optional instructions, as per 1149.1
     "CLAMP   (0100), " &
```

```
     "HIGHZ   (1101), " &
     "INTEST  (1110), " &
     "IDCODE  (0001)";

attribute INSTRUCTION_CAPTURE of Kitchen_Sink_2_2 : entity is "0001";

attribute IDCODE_REGISTER of Kitchen_Sink_2_2 : entity is
     "XXXX" &             -- version
     "0000000000000000" & -- part number
     "10101010101" &      -- manufacturer id
     "1";

attribute REGISTER_ACCESS of Kitchen_Sink_2_2 : entity is
  -- access to mandatory registers, as per 1149.1
     "BOUNDARY (EXTEST, PRELOAD, SAMPLE), " &
     "BYPASS (BYPASS), " &
     "BOUNDARY (INTEST), " &
  -- access to mandatory registers, as per 1149.4
  -- = register BOUNDARY must be accessed by instruction PROBE
     "BOUNDARY (PROBE), " &
  -- access to optional register, as per 1149.1
     "DEVICE_ID (IDCODE)";

attribute BOUNDARY_LENGTH of Kitchen_Sink_2_2 : entity is 47;

attribute BOUNDARY_REGISTER of Kitchen_Sink_2_2 : entity is

  -- following cells (2) are for the digital pins
  -- num cell port function safe [ccell disval rslt]
     "0  (BC_1,    A, input,        x), " &
     "1  (BC_1,    B, input,        x), " &

  -- following cells (6) are for the digital differential pins
  -- num cell port function safe [ccell disval rslt]
     "2  (BC_1,   D1, input,        x), " &
     "3  (BC_1,  D1N, input,        x), " &
     "4  (BC_1,    *, internal,     x), " &  -- D1:D1N SE
     "5  (BC_1,   D2, input,        x), " &
     "6  (BC_1,  D2N, input,        x), " &
     "7  (BC_4,    *, internal,     x), " &  -- D2:D2N SE

  -- following cells (4) are TBIC  base controls
  -- num cell port function safe [ccell disval rslt]
     "8  (BC_1,    *, internal,     0), " &          -- Ca
     "9  (BC_1,    *, control,      0), " &          -- Co
     "10 (BC_7,  AT1, bidir,        0,  9, 0, Z), " & -- D1
     "11 (BC_7,  AT2, bidir,        0,  9, 0, Z), " & -- D2

  -- following cells (4) are TBIC  extension controls
  -- num cell port function safe
     "12 (BC_1,    *, internal,     0), " &          -- D1
     "13 (BC_1,    *, internal,     0), " &          -- D2

  -- following cells (4) are TBICN base controls
  -- num cell port function safe [ccell disval rslt]
     "14 (BC_1,    *, internal,     0), " &          -- Ca
     "15 (BC_1,    *, control,      0), " &          -- Co
     "16 (BC_7, AT1N, bidir,        0, 15, 0, Z), " & -- D1
     "17 (BC_7, AT2N, bidir,        0, 15, 0, Z), " & -- D2
```

```
-- following cells (2) are TBIC  extension controls
-- num cell port function safe
   "18 (BC_1,    *, internal,     0), " &           -- D1
   "19 (BC_1,    *, internal,     0), " &           -- D2

-- following cells (2) are TBICN extension controls
-- num cell port function safe
   "20 (BC_1,    *, internal,     0), " &           -- D1
   "21 (BC_1,    *, internal,     0), " &           -- D1

-- following cells (4) control the analog signal W
-- num cell port function safe [ccell disval rslt]
   "22 (BC_1,    *, control,      0), " &           -- C
   "23 (BC_7,    W, bidir,        x, 22, 0, Z), " & -- D
   "24 (BC_1,    *, internal,     0), " &           -- B1
   "25 (BC_1,    *, internal,     0), " &           -- B2

-- following cells (4) control the analog signal Y
-- num cell port function safe [ccell disval rslt]
   "26 (BC_1,    *, control,      0), " &           -- C
   "27 (BC_7,    Y, bidir,        x, 26, 0, Z), " & -- D
   "28 (BC_1,    *, internal,     0), " &           -- B1
   "29 (BC_1,    *, internal,     0), " &           -- B2

-- following cells (4) control the analog differential signal X1
-- num cell port function safe [ccell disval rslt]
   "30 (BC_1,    *, control,      0), " &           -- C
   "31 (BC_7,   X1, bidir,        x, 30, 0, Z), " & -- D
   "32 (BC_1,    *, internal,     0), " &           -- B1
   "33 (BC_1,    *, internal,     0), " &           -- B2

-- following cells (4) control the analog differential signal X1N
-- num cell port function safe [ccell disval rslt]
   "34 (BC_1,    *, control,      0), " &           -- C
   "35 (BC_7,  X1N, bidir,        x, 34, 0, Z), " & -- D
   "36 (BC_1,    *, internal,     0), " &           -- B1
   "37 (BC_1,    *, internal,     0), " &           -- B2

-- following cells (4) control the analog differential signal X2
-- num cell port function safe [ccell disval rslt]
   "38 (BC_1,    *, control,      0), " &           -- C
   "39 (BC_7,   X2, bidir,        x, 38, 0, Z), " & -- D
   "40 (BC_1,    *, internal,     0), " &           -- B1
   "41 (BC_1,    *, internal,     0), " &           -- B2

-- following cells (4) control the analog differential signal X2N
-- num cell port function safe [ccell disval rslt]
   "42 (BC_1,    *, control,      0), " &           -- C
   "43 (BC_7,  X2N, bidir,        x, 42, 0, Z), " & -- D
   "44 (BC_1,    *, internal,     0), " &           -- B1
   "45 (BC_1,    *, internal,     0), " &           -- B2

-- following cell  (1) is a "dummy"
   "46 (BC_1,    *, internal,     0)";
```

```
-- BSDL extensions follow, as per 1149.1
-- MST attributes declared in package "Std_1149_4_2005", as per 1149.4

-- component conformance, as per 1149.4
attribute MST_Component_Conformance of Kitchen_Sink_2_2 : entity is
     "STD_1149_4_1999";

-- ATAP  port identification, as per 1149.4
attribute MST_ATAP_AT1  of Kitchen_Sink_2_2 : entity is "AT1";
attribute MST_ATAP_AT2  of Kitchen_Sink_2_2 : entity is "AT2";

-- ATAPN port identification, as per 1149.4
-- = only required for optional differential ATAP
attribute MST_ATAP_AT1N of Kitchen_Sink_2_2 : entity is "AT1N";
attribute MST_ATAP_AT2N of Kitchen_Sink_2_2 : entity is "AT2N";

-- TBIC  register, as per 1149.4
-- = ref tables 1 and 2
attribute MST_TBIC_Register  of Kitchen_Sink_2_2 : entity is
  -- Ca_num Co_num
     " 8,  9 : " &
  -- { partition_name D1_num D2_num}
     " IATB0 (10, 11), " &
     " IATB1 (12, 13), " &
     " IATB2 (18, 19)";

-- TBICN register, as per 1149.4
-- = ref tables 1 and 2
attribute MST_TBICN_Register of Kitchen_Sink_2_2 : entity is
  -- Ca_num Co_num
     "14, 15 : " &
  -- {Npartition_name D1_num D2_num}
     "NIATB1 (16, 17), " &
     "NIATB2 (20, 21)";

attribute MST_Diff_Pins_Table of Kitchen_Sink_2_2 : entity is
  -- DBMs at single-ended side of differential drivers/receivers
  -- representative_port associated_port num
     "D1 : D1N ( 4), " &
     "D2 : D2N ( 7)";

attribute MST_ABM_Pins_Table of Kitchen_Sink_2_2 : entity is
  -- ABMs, as per 1149.4 = ref tables 6, 7, and 8
  -- port partition_name C_num D_num B1_num B2_num
     "W   (  IATB0: 22, 23, 24, 25 ), " &
     "Y   (  IATB0: 26, 27, 28, 29 ), " &
     "X1  (  IATB1: 30, 31, 32, 33 ), " &
     "X1N ( NIATB1: 34, 35, 36, 37 ), " &
     "X2  (  IATB2: 38, 39, 40, 41 ), " &
     "X2N ( NIATB2: 42, 43, 44, 45 )";

end Kitchen_Sink_2_2;
```