IEEE 1149.4 Mixed-Signal Test Bus Working Group Meeting Minutes

for

September 25th, 2008
12:00 – 1:00 PM PDT

Meeting Agenda:

Time	Topic	Responsibility
12:00 – 1:10 PM	1. Review meeting minutes for August 11th, 2008 2. Review standard draft - Twin Group - Differential Digital Port Grouping - Other updates 3. Other issues.	All All All
1:10 PM	Meeting adjourned	Bambang

Meeting Attendees:

Name	Company
Adam Cron	Synopsys
Ken Parker	Agilent Technologies
Bambang Suparjo	Mentor Graphics

1. Review meeting minutes for August 11th, 2008.

The meeting minutes for August 11th, 2008 have been approved, suggested by Ken and seconded by Adam Cron.

2. Review Standard Draft (version D10)

a. Twin Group

This issue is referring to the curly brackets used in the definition of <MST group table>.

<MST port grouping statement> ::= **attribute MST_PORT_GROUPING of**
<component name> **: entity is** <MST group table string> **;**
<MST group table string> ::= **"** <MST group table> **"**
<MST group table> ::= <MST twin group entry> **{ ,** <MST twin group entry> **}**
<MST twin group entry> ::= <MST twin group type> **(**<MST twin group record list>**)**
<MST twin group type> ::= **DIFFERENTIAL_DIGITAL | DIFFERENTIAL_ANALOG**
<MST twin group record list> ::= <MST twin group record> { **,** <MST twin group record> }
<MST twin group record> ::= **(** <twin group> **:** <MST differential capture cell list> **)**
<MST differential capture cell list> ::=
<MST differential capture cell> { **,** <MST differential capture cell> }
<MST differential capture cell> ::= <integer>

It is clear that we have a syntax for MST Twin Groups that is a bit overly-rich for what we intended. Since there are only two types of <MST twin group type> entries, the curly brackets should be replaced with square brackets [ ] characters. This proposal would limit some of this richness, but still allow for syntax well beyond our examples. The change has been made in the draft.

b. Differential Digital Port Grouping.

The relevant emails have been reviewed but having difficulty to understand the following statement from Adam Ley:

"I would expect that ALL pins with dot 4 facilities, whether truly analog or essentially digital, will be declared with port type inout - will have full bidir capability as expressed in the boundary register attribute and thus will NOT appear in the <port grouping statement>."

It has been suggested to discuss this issue in the next teleconference.

c. Other updates.

This is regarding an assignment note that Adam Cron needs to do in page 81 related to boundary scan cells for digital differential pair especially for those cells that violate 1149.1. A new paragraph (shown below) has been added in page 81:

New resources specifically allowed and stipulated by this Standard (7.2.1.1 a), for example) pertain to digital differential pins. Refer to Figure 56 in Clause 10.4.4.5.3 for detail on the appropriate syntax.

3. Other issues

The next teleconference will be on October 3rd, 8-9 AM Pacific Time.

4. The meeting adjourned at 1:10 PM PDT